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UTILITY PATENT APPLICATION TRANSMITTAL *(Only for new nonprovisional applications under 37 CFR § 1.53(b))*	Attorney Docket No.	1744.0450003
	First Inventor or Application Identifier	David F. SORRELLS
	Title	Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal
	Express Mail Label No.	

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO· Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ * Fee Transmittal Form *(e.g., PTO/SB/17)*
   (Submit an original, and a duplicate for fee processing)

2. ☒ Specification   [Total Pages 134]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure

3. ☒ Drawings (35 U.S.C. 113)   [Total Sheets 134]

4. ☐ Oath or Declaration   [Total Pages _____]

   a. ☐ Newly executed (original or copy)

   b ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      [Note Box 5 below]

      i. ☐ <u>DELETION OF INVENTOR(S)</u>
         Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1 33(b).

5. ☐ Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein

6. ☐ Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*

   a. ☐ Computer Readable Copy

   b. ☐ Paper Copy (identical to computer copy)

   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))

9 ☐ 37 CFR 3.73(b) Statement   ☐ Power of Attorney
   (when there is an assignee)

10 ☐ English Translation Document *(if applicable)*

11 ☐ Information Disclosure   ☐ Copies of IDS Citations
   Statement (IDS)/PTO-1449

12 ☐ Preliminary Amendment

13 ☒ Return Receipt Postcard (MPEP 503)
   (Should be specifically itemized)

14 ☐ *Small Entity Statement(s)   ☐ Statement filed in prior
   (PTO/SB/09-12)   application, Status still proper and desired

15 ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16 ☒ Other   37 C.F.R § 1.136(a)(3) Authorization

   ☐ Other

*NOTE FOR ITEMS 1 & 14 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R § 1 27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. §1.28).

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

☐ Continuation   ☐ Divisional   ☐Continuation-in-Part (CIP) of prior application No: ____/_____

Prior application information: Examiner _____   *Group/Art Unit:* _____

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March 14, 2000

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Assistant Commissioner for Patents
Washington, D.C. 20231

Box Patent Application

Sir:

    Re: U.S. Non-Provisional Utility Patent Application under 37 C.F.R. § 1.53(b)
Appl. No. To be assigned; Filed: March 14, 2000
For: **Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal**
Inventors: David F. Sorrells, Michael J. Bultman, Robert W. Cook, Richard C. Looke, Charley D. Moses, Jr., Gregory S. Rawlins, and Michael W. Rawlins
Our Ref: 1744.0450003

Sir:

    The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1.   PTO Utility Patent Application Transmittal Form (PTO/SB/05);

2.   U.S. Utility Patent Application entitled:

Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal

and naming as inventors:

David F. Sorrells, Michael J. Bultman, Robert W. Cook, Richard C. Looke, Charley D. Moses, Jr., Gregory S. Rawlins, and Michael W. Rawlins

the application consisting of:

a. A specification containing:

  i. 108 pages of description prior to the claims;

  ii. 25 pages of claims (95 claims);

  iii. a one (1) page abstract;

b. One-hundred and thirty-four (134) sheets of drawings: (Figures 1A-D, 2A, 2B, 3-14, 15A-F, 16-19, 20A, 20A-1, 20B-F, 21, 22A-F, 23A-F,24A-J, 25A, 25B, 26A-D, 27A-J, 28A, 28B, 29, 30A-C, 31A, 31B, 32, 33, 34A, 34B, 35A, 35B, 36, 37A-F, 38-51, 52A-Z, 53A-C, 54A-C, 55A-D, 56A-D, 57, 58A-C, 59-67, 68A, 68B, 69A, 69B, 70A-R, 71-73, and 74A-E);

3. PTO Fee Transmittal Form PTO/SB/17 (in duplicate);

4. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3)(in duplicate);

5. Our check No. 26910 for $2,664.00 to cover:

  $ 690.00 filing fee for patent application;
  $1,350.00 fee for claims in excess of twenty;
  $ 624.00 fee for excess independent claims; and

6. Two (2) return postcards.

It is respectfully requested that, of the two attached postcards, one be stamped with the filing date of these documents and returned to our courier, and the other, prepaid postcard, be stamped with the filing date and unofficial application number and returned as soon as possible.

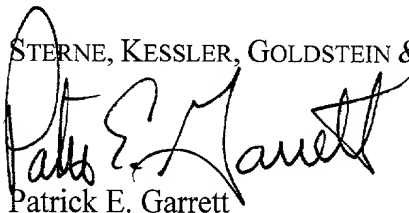Assistant Commissioner for Patents
March 14, 2000
Page 3

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. A duplicate copy of this letter is enclosed.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Patrick E. Garrett
Attorney for Applicants
Registration No. 39,987

0450003 pto

Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal

Inventors:

David F. Sorrells
Michael J. Bultman
Robert W. Cook
Richard C. Looke
Charley D. Moses, Jr.
Gregory S. Rawlins
Michael W. Rawlins

This application claims priority to the following: U.S. Provisional Application No.60/177,381, filed on 1/24/00; U.S. Provisional Application No.60/171,502, filed 12/22/1999; U.S. Provisional Application No. 60/177,705, filed on 01/24/2000; U.S. Provisional Application No. 60/129,839, filed on 04/16/1999; U.S Provisional Application No. 60/158,047,filed on 10/07/1999; U.S. Provisional Application No.60/171,349, filed on 12/21/1999, U S. Provisional Application No.60/177,702, filed on 01/24/2000; U.S. Provisional Application No. 60/180,667, filed on 2/7/00; and U.S. Provisional Application No.60/171,496, filed on 12/22/99; all of which are incorporated by reference herein in their entireties.

Cross-Reference to Other Applications

The following applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

"Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998;

"Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998;

1744.0450003

"Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998;

"Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed October 21, 1998;

"Universal Frequency Translation, and Applications of Same," Ser. No. 09/176,027, filed October 21, 1998;

"Applications of Universal Frequency Translation," filed March 3, 1999, Ser. No. 09/261,129, filed 3/3/1999;

"Matched Filter Characterization and Implementation of Universal Frequency Translation Method and Apparatus," Attorney Docket No. 1744.0920000, filed 3/9/99;

"Spread Spectrum Applications of Universal Frequency Translation," Attorney Docket No. 1744,0450002; and

"DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Attorney Docket No. 1744.0880000.

Background of the Invention

Field of the Invention

The present invention is generally related to frequency up-conversion of a baseband signal, and applications of same. The invention is also directed to embodiments for frequency down-conversion, and to transceivers.

Related Art

Various communication components and systems exist for performing frequency up-conversion and down-conversion of electromagnetic signals.

Summary of the Invention

The present invention is related to up-converting a baseband signal, and applications of same. Such applications include, but are not limited to, up-converting a spread spectrum signal directly from baseband to radio frequency (RF) without utilizing any intermediate frequency (IF) processing. The invention is also related to frequency down-conversion.

In embodiments, the invention differentially samples a baseband signal according to first and second control signals, resulting in a harmonically rich signal. The harmonically rich signal contains multiple harmonic images that each contain the necessary amplitude, frequency, and/or phase information to reconstruct the baseband signal. The harmonic images in the harmonically rich signal repeat at the harmonics of the sampling frequency ($1/T_S$) that are associated with the first and second control signals. In other words, the sampling is performed sub-harmonically according to the control signals. Additionally, the control signals include pulses that have an associated pulse width T_A that is established to improve energy transfer to a desired harmonic image in the harmonically rich signal. The desired harmonic image can optionally be selected using a bandpass filter for transmission over a communications medium.

In operation, the invention converts the input baseband signal from a (single-ended) input into a differential baseband signal having first and second components. The first differential component is substantially similar to the input baseband signal, and the second differential component is an inverted version of the input baseband signal. The first differential component is sampled according to the first control signal, resulting in a first harmonically rich signal. Likewise, the second differential component is sampled according to the second control signal, resulting in a second

harmonically rich signal. The first and second harmonically rich signals are combined to generate the output harmonically rich signal.

The sampling modules that perform the differentially sampling can be configured in a series or shunt configuration. In the series configuration, the baseband input is received at one port of the sampling module, and is gated to a second port of the sampling module, to generate the harmonically rich signal at the second port of the sampling module. In the shunt configuration, the baseband input is received at one port of the sampling module and is periodically shunted to ground at the second port of the sampling module, according to the control signal. Therefore, in the shunt configuration, the harmonically rich signal is generated at the first port of the sampling module and coexists with the baseband input signal at the first port.

The first control signal and second control signals that control the sampling process are phase shifted relative to one another. In embodiments of the invention, the phase-shift is 180 degree in reference to a master clock signal, although the invention includes other phase shift values. Therefore, the sampling modules alternately sample the differential components of the baseband signal. Additionally as mentioned above, the first and second control signals include pulses having a pulse width T_A that is established to improve energy transfer to a desired harmonic in the harmonically rich signal during the sampling process. More specifically, the pulse width T_A is a non-negligible fraction of a period associated with a desired harmonic of interest. In an embodiment, the pulse width T_A is one-half of a period of the harmonic of interest. Additionally, in an embodiment, the frequency of the pulses in both the first and second control signal are a sub-harmonic frequency of the output signal.

In further embodiments, the invention minimizes DC offset voltages between the sampling modules during the differential sampling. In the serial configuration, this is accomplished by distributing a reference voltage to the input and output of the sampling modules. The result of minimizing (or preventing) DC offset voltages is that carrier insertion is minimized in the harmonics of the harmonically rich signal. In many

1744.0450003

transmit applications, carrier insertion is undesirable because the information to be transmitted is carried in the sidebands, and any energy at the carrier frequency is wasted. Alternatively, some transmit applications require sufficient carrier insertion for coherent demodulation of the transmitted signal at the receiver. In these applications, the invention can be configured to generate offset voltages between sampling modules, thereby causing carrier insertion in the harmonics of the harmonically rich signal.

An advantage is that embodiments of the invention up-convert a baseband signal directly from baseband-to-RF without any IF processing, while still meeting the spectral growth requirements of the most demanding communications standards. (Other embodiments may employ if processing.) For example, in an I Q configuration, the invention can up-convert a CDMA spread spectrum signal directly from baseband-to-RF, and still meet the CDMA IS-95 figure-of-merit and spectral growth requirements. In other words, the invention is sufficiently linear and efficient during the up-conversion process that no IF filtering or amplification is required to meet the IS-95 figure-of-merit and spectral growth requirements. As a result, the entire IF chain in a conventional CDMA transmitter configuration can be eliminated, including the expensive and hard to integrate SAW filter. Since the SAW filter is eliminated, substantial portions of a CDMA transmitter that incorporate the invention can be integrated onto a single CMOS chip that uses a standard CMOS process, although the invention is not limited to this example application.

Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. The drawing in which an element first appears is typically indicated by the leftmost character(s) and/or digit(s) in the corresponding reference number.

Brief Description of the Figures

The present invention will be described with reference to the accompanying drawings, wherein:

FIG. 1A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention;

FIG. 1C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention;

FIG. 1D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 2A is a block diagram of a universal frequency translation (UFT) module according to embodiments of the invention;

FIG. 2B is a block diagram of a universal frequency translation (UFT) module according to embodiments of the invention;

FIG. 3 is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 4 is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention;

FIG. 5 is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention;

FIGS. 6A-6I illustrate example waveforms used to describe the operation of the UFU module;

FIG. 7 illustrates a UFT module used in a receiver according to an embodiment of the invention;

FIG. 8 illustrates a UFT module used in a transmitter according to an embodiment of the invention;

1744.0450003

FIG. 9 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using a UFT module of the invention;

FIG. 10 illustrates a transceiver according to an embodiment of the invention;

FIG. 11 illustrates a transceiver according to an alternative embodiment of the invention;

FIG. 12 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention;

FIG. 13 illustrates a UFT module used in a unified down-conversion and filtering (UDF) module according to an embodiment of the invention;

FIG. 14 illustrates an example receiver implemented using a UDF module according to an embodiment of the invention;

FIGS. 15A-15F illustrate example applications of the UDF module according to embodiments of the invention;

FIG. 16 illustrates an environment comprising a transmitter and a receiver, each of which may be implemented using enhanced signal reception (ESR) components of the invention, wherein the receiver may be further implemented using one or more UFD modules of the invention;

FIG. 17 illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention;

FIG. 18 is a table of example values at nodes in the UDF module of FIG 17;

FIG. 19 is a detailed diagram of an example UDF module according to an embodiment of the invention;

FIGS. 20A and 20A-1 are example aliasing modules according to embodiments of the invention;

FIGS. 20B-20F are example waveforms used to describe the operation of the aliasing modules of FIGS. 20A and 20A-1;

1744.0450003

FIG. 21 illustrates an enhanced signal reception system according to an embodiment of the invention;

FIGS. 22A-22F are example waveforms used to describe the system of FIG. 21;

FIG. 23A illustrates an example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 23B and 23C are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 23D illustrates another example transmitter in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 23E and 23F are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIG. 24A illustrates an example receiver in an enhanced signal reception system according to an embodiment of the invention;

FIGS. 24B-24J are example waveforms used to further describe the enhanced signal reception system according to an embodiment of the invention;

FIGs. 25A-B illustrate carrier insertion;

FIGs. 26A-C illustrate a balanced transmitter 2602 according to an embodiment of the present invention;

FIG. 26B-C illustrate example waveforms that are associated with the balanced transmitter 2602 according to an embodiment of the present invention;

FIG. 26D illustrates example FET configurations of the balanced transmitter 2602;

FIGs.27A-I illustrate various example timing diagrams associated with the transmitter 2602;

FIG. 27J illustrates an example frequency spectrum associated with the modulator 2604;

FIG. 28A illustrate a balanced modulator 2802 configured for carrier insertion according to embodiments of the present invention;

FIG. 28B illustrates example signal diagrams associated with the balanced transmitter 2802 according to embodiments of the invention;

FIG. 29 illustrates an I Q balanced transmitter 2920 according to embodiments of the present invention;

FIGs. 30A-C illustrate various example signal diagrams associated with the balanced transmitter 2920 in FIG. 29;

FIG. 31A illustrates an I Q balanced transmitter 3108 according to embodiments of the invention;

FIG. 31B illustrates an I Q balanced modulator 3118 according to embodiments of the invention;

FIG. 32 illustrates an I Q balanced modulator 3202 configured for carrier insertion according to embodiments of the invention;

FIG. 33 illustrates an I Q balanced modulator 3302 configured for carrier insertion according to embodiments of the invention;

FIGs. 34A-B illustrate various input configurations for the balanced transmitter 2920 according to embodiments of the present invention;

FIGs. 35A-B illustrate sidelobe requirements according to the IS-95 CDMA specification;

FIG. 36 illustrates a conventional CDMA transmitter 3600;

FIG. 37A illustrates a CDMA transmitter 3700 according to embodiments of the present invention;

FIGs. 37B-E illustrate various example signal diagrams according to embodiments of the present invention;

FIG. 37F illustrates a CDMA transmitter 3720 according to embodiments of the present invention;

1744 0450003

FIG. 38 illustrates a CDMA transmitter utilizing a CMOS chip according to embodiments of the present invention;

FIG. 39 illustrates an example test set 3900;

FIGs. 40-52Z illustrate various example test results from testing the modulator 2910 in the test set 3900;

FIGs. 53A-C illustrate a transmitter 5300 and associated signal diagrams according to embodiments of the present invention;

FIGs. 54A-B illustrate a transmitter 5400 and associated signal diagrams according to embodiments of the present invention;

FIG. 54C illustrates a transmitter 5430 according to embodiments of the invention;

FIGs. 55A-D illustrates various implementation circuits for the modulator 2910 according to embodiments of the present invention;

FIG. 56A illustrate a transmitter 5600 according to embodiments of the present invention;

FIGs. 56B-C illustrate various frequency spectrums that are associated with the transmitter 5600;

FIG. 56D illustrates a FET configuration for the modulator 5600;

FIG 57 illustrates a IQ transmitter 5700 according to embodiments of the present invention;

FIGs. 58A-C illustrate various frequency spectrums that are associated with the IQ transmitter 5700;

FIG. 59 illustrates an IQ transmitter 5900 according to embodiments of the present invention;

FIG. 60 illustrates an IQ transmitter 6000 according to embodiments of the present invention;

FIG. 61 illustrates an IQ transmitter 6100 according to embodiments of the invention;

FIG. 62 illustrates a flowchart 6200 that is associated with the transmitter 2602 in the FIG. 26A according to an embodiment of the invention;

FIG. 63 illustrates a flowchart 6300 that further defines the flowchart 6200 in the FIG. 62, and is associated with the transmitter 2602 according to an embodiment of the invention;

FIG. 64 illustrates a flowchart 6400 that further defines the flowchart 6200 in the FIG. 63 and is associated with the transmitter 6400 according to an embodiment of the invention;

FIG. 65 illustrates the flowchart 6500 that is associated with the transmitter 2920 in the FIG. 29 according to an embodiment of the invention;

FIG. 66 illustrates a flowchart 6600 that is associated with the transmitter 5700 according to an embodiment of the invention;

FIG. 67 illustrates a flowchart 6700 that is associated with the spread spectrum transmitter 5300 in FIG. 53A according to an embodiment of the invention;

FIGs. 68A and FIG. 68B illustrate a flowchart 6800 that is associated with an IQ spread spectrum modulator 6100 in FIG. 61 according to an embodiment of the invention;

FIGs. 69A and FIG. 69B illustrate a flowchart 6900 that is associated with an IQ spread spectrum transmitter 5300 in FIG. 54A according to an embodiment of the invention;

FIG. 70A illustrates an IQ receiver having shunt UFT modules according to embodiments of the invention;

FIG. 70B illustrates control signal generator embodiments for receiver 7000 according to embodiments of the invention;

FIGs. 70C-D illustrate various control signal waveforms according to embodiments of the invention;

FIG. 70E illustrates an example IQ modulation receiver embodiment according to embodiments of the invention;

1744.0450003

FIGs. 70F-P illustrate example waveforms that are representative of the IQ receiver in FIG. 70E;

FIGs. 70Q-R illustrate single channel receiver embodiments according to embodiments of the invention;

FIG. 71 illustrates a transceiver 7100 according to embodiments of the present invention;

FIG. 72 illustrates a transceiver 7200 according to embodiments of the present invention;

FIG. 73 illustrates a flowchart 7300 that is associated with the CDMA transmitter 3720 in FIG. 37 according to an embodiment of the invention;

FIG. 74A illustrates various pulse generators according to embodiments of the invention;

FIGs. 74B-C illustrate various example signal diagrams associated with the pulse generator in FIG. 74A, according to embodiments of the invention; and

FIGs. 74D-E illustrate various additional pulse generators according to embodiments of the invention.

Detailed Description of the Preferred Embodiments

Table of Contents

1744.0450003

1. *Universal Frequency Translation*

The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

FIG. 1A illustrates a universal frequency translation (UFT) module 102 according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

As indicated by the example of FIG. 1A, some embodiments of the UFT module 102 include three ports (nodes), designated in FIG. 1A as Port 1, Port 2, and Port 3. Other UFT embodiments include other than three ports.

Generally, the UFT module 102 (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module 102 (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

An example embodiment of the UFT module 103 is generally illustrated in FIG. 1B. Generally, the UFT module 103 includes a switch 106 controlled by a control signal 108. The switch 106 is said to be a controlled switch.

As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. 2 illustrates an example UFT module 202. The example UFT module 202 includes a diode 204 having two ports, designated as Port 1 and Port 2/3. This embodiment does not include a third port, as indicated by the dotted line around the "Port 3" label. FIG. 2B illustrates a second example UFT module 208 having a FET 210 whose gate is controlled by the control signal.

The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

For example, a UFT module 115 can be used in a universal frequency down-conversion (UFD) module 114, an example of which is shown in FIG. 1C. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal.

As another example, as shown in FIG. 1D, a UFT module 117 can be used in a universal frequency up-conversion (UFU) module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal.

These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

2. *Frequency Down-conversion*

The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in co-pending U.S. Patent Application entitled "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, the full disclosure of which is incorporated herein by reference. A relevant portion of the above mentioned patent application is summarized below to describe down-converting an input signal to

produce a down-converted signal that exists at a lower frequency or a baseband signal.

FIG. 20A illustrates an aliasing module 2000 (one embodiment of a UFD module) for down-conversion using a universal frequency translation (UFT) module 2002, which down-converts an EM input signal 2004. In particular embodiments, aliasing module 2000 includes a switch 2008 and a capacitor 2010. The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch 2008 is in series with input signal 2004 and capacitor 2010 is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. 20A-1), the capacitor 2010 is in series with the input signal 2004 and the switch 2008 is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module 2000 with UFT module 2002 can be easily tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal 2004.

In one implementation, aliasing module 2000 down-converts the input signal 2004 to an intermediate frequency (IF) signal. In another implementation, the aliasing module 2000 down-converts the input signal 2004 to a demodulated baseband signal. In yet another implementation, the input signal 2004 is a frequency modulated (FM) signal, and the aliasing module 2000 down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

In an embodiment, the control signal 2006 includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal 2004. In this embodiment, the control signal 2006 is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal 2004. Preferably, the frequency of control signal 2006 is much less than the input signal 2004.

1744.0450003

A train of pulses 2018 as shown in FIG. 20D controls the switch 2008 to alias the input signal 2004 with the control signal 2006 to generate a down-converted output signal 2012. More specifically, in an embodiment, switch 2008 closes on a first edge of each pulse 2020 of FIG. 20D and opens on a second edge of each pulse. When the switch 2008 is closed, the input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal to the capacitor 2010. The charge stored during successive pulses forms down-converted output signal 2012.

Exemplary waveforms are shown in FIGS. 20B-20F.

FIG. 20B illustrates an analog amplitude modulated (AM) carrier signal 2014 that is an example of input signal 2004. For illustrative purposes, in FIG. 20C, an analog AM carrier signal portion 2016 illustrates a portion of the analog AM carrier signal 2014 on an expanded time scale. The analog AM carrier signal portion 2016 illustrates the analog AM carrier signal 2014 from time t_0 to time t_1.

FIG. 20D illustrates an exemplary aliasing signal 2018 that is an example of control signal 2006. Aliasing signal 2018 is on approximately the same time scale as the analog AM carrier signal portion 2016. In the example shown in FIG. 20D, the aliasing signal 2018 includes a train of pulses 2020 having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses 2020 repeat at an aliasing rate, or pulse repetition rate of aliasing signal 2018. The aliasing rate is determined as described below, and further described in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000.

As noted above, the train of pulses 2020 (i.e., control signal 2006) control the switch 2008 to alias the analog AM carrier signal 2016 (i.e., input signal 2004) at the aliasing rate of the aliasing signal 2018. Specifically, in this embodiment, the switch 2008 closes on a first edge of each pulse and opens on a second edge of each pulse.

When the switch 2008 is closed, input signal 2004 is coupled to the capacitor 2010, and charge is transferred from the input signal 2004 to the capacitor 2010. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples 2022 form down-converted signal portion 2024 (FIG. 20E) that

5   corresponds to the analog AM carrier signal portion 2016 (FIG. 20C) and the train of pulses 2020 (FIG. 20D). The charge stored during successive under-samples of AM carrier signal 2014 form the down-converted signal 2024 (FIG. 20E) that is an example of down-converted output signal 2012 (FIG. 20A). In FIG. 20F, a demodulated baseband signal 2026 represents the demodulated baseband signal 2024

10   after filtering on a compressed time scale. As illustrated, down-converted signal 2026 has substantially the same "amplitude envelope" as AM carrier signal 2014. Therefore, FIGS. 20B-20F illustrate down-conversion of AM carrier signal 2014.

The waveforms shown in FIGS. 20B-20F are discussed herein for illustrative purposes only, and are not limiting. Additional exemplary time domain and frequency

15   domain drawings, and exemplary methods and systems of the invention relating thereto, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No.09/176,022, Attorney Docket Number 1744.0010000.

The aliasing rate of control signal 2006 determines whether the input signal

20   2004 is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal 2004, the aliasing rate of the control signal 2006, and the down-converted output signal 2012 are illustrated below:

25   (Freq. of input signal 2004) = n•(Freq. of control signal 2006) ±
(Freq. of down-converted output signal 2012)

For the examples contained herein, only the "+" condition will be discussed. The value of n represents a harmonic or sub-harmonic of input signal 2004 (e.g., $n = 0.5$, 1, 2, 3, . . .).

When the aliasing rate of control signal 2006 is off-set from the frequency of input signal 2004, or off-set from a harmonic or sub-harmonic thereof, input signal 2004 is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal 2004. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal 2006 would be calculated as follows:

$$(\text{Freq}_{input} - \text{Freq}_{IF})/n = \text{Freq}_{control}$$
$$(901 \text{ MHZ} - 1 \text{ MHZ})/n = 900/n$$

For $n = 0.5$, 1, 2, 3, 4, etc., the frequency of the control signal 2006 would be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating down-conversion of analog and digital AM, PM and FM signals to IF signals, and exemplary methods and systems thereof, are disclosed in co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000.

Alternatively, when the aliasing rate of the control signal 2006 is substantially equal to the frequency of the input signal 2004, or substantially equal to a harmonic or sub-harmonic thereof, input signal 2004 is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-

sampling pulses occur at the same point of subsequent cycles of the input signal 2004. As a result, the under-samples form a constant output baseband signal. If the input signal 2004 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHZ input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal 2006 would be calculated as follows:

$$(Freq_{input} - Freq_{IF})/n = Freq_{control}$$
$$(900\ MHZ - 0\ MHZ)/n = 900\ MHZ/n$$

For n = 0.5, 1, 2, 3, 4, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

Exemplary time domain and frequency domain drawings, illustrating direct down-conversion of analog and digital AM and PM signals to demodulated baseband signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. _09/176,022, Attorney Docket Number 1744.0010000.

Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1 + F_2) \div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal 2006 would be calculated as follows:

Frequency of the input $= (F_1 + F_2) \div 2$

$\qquad = (899\ MHZ + 901\ MHZ) \div 2$

$\qquad = 900\ MHZ$

Frequency of the down-converted signal = 0 (i.e., baseband)

$(Freq_{input} - Freq_{IF})/n = Freq_{control}$

$(900\ MHZ - 0\ MHZ)/n = 900\ MHZ/n$

For $n = 0.5$, 1, 2, 3, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2.

As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHZ and F_2 equal to 901 MHZ, to an ASK signal, the aliasing rate of the control signal 2006 should be substantially equal to:

$(900\ MHZ - 0\ MHZ)/n = 900\ MHZ/n$, or

$(901\ MHZ - 0\ MHZ)/n = 901\ MHZ/n$.

For the former case of 900 MHZ/n, and for $n = 0.5$, 1, 2, 3, 4, etc., the frequency of the control signal 2006 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. For the latter case of 901 MHZ/n, and for $n = 0.5$, 1, 2, 3, 4, etc., the frequency of the control signal 2006 should be substantially equal to 1.802 GHz, 901 MHZ, 450.5 MHZ, 300.333 MHZ, 225.25 MHZ, etc. The

frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHZ).

Exemplary time domain and frequency domain drawings, illustrating down-conversion of FM signals to non-FM signals, and exemplary methods and systems thereof, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000.

In an embodiment, the pulses of the control signal 2006 have negligible apertures that tend towards zero. This makes the UFT module 2002 a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

In another embodiment, the pulses of the control signal 2006 have non-negligible apertures that tend away from zero. This makes the UFT module 2002 a lower input impedance device. This allows the lower input impedance of the UFT module 2002 to be substantially matched with a source impedance of the input signal 2004. This also improves the energy transfer from the input signal 2004 to the down-converted output signal 2012, and hence the efficiency and signal to noise (s/n) ratio of UFT module 2002.

Exemplary systems and methods for generating and optimizing the control signal 2006, and for otherwise improving energy transfer and s/n ratio, are disclosed in the co-pending U.S. Patent Application entitled "Method and System for Down-converting Electromagnetic Signals," Application No. 09/176,022, Attorney Docket Number 1744.0010000.

3.   *Frequency Up-conversion Using Universal Frequency Translation*

The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

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An example frequency up-conversion system 300 is illustrated in FIG. 3. The frequency up-conversion system 300 is now described.

An input signal 302 (designated as "Control Signal" in FIG. 3) is accepted by a switch module 304. For purposes of example only, assume that the input signal 302 is a FM input signal 606, an example of which is shown in FIG. 6C. FM input signal 606 may have been generated by modulating information signal 602 onto oscillating signal 604 (FIGS. 6A and 6B). It should be understood that the invention is not limited to this embodiment. The information signal 602 can be analog, digital, or any combination thereof, and any modulation scheme can be used.

The output of switch module 304 is a harmonically rich signal 306, shown for example in FIG. 6D as a harmonically rich signal 608. The harmonically rich signal 608 has a continuous and periodic waveform.

FIG. 6E is an expanded view of two sections of harmonically rich signal 608, section 610 and section 612. The harmonically rich signal 608 may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular waveform" is used to refer to waveforms that are substantially rectangular. In a similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

Harmonically rich signal 608 is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal 608. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. 6F and FIG. 6G show separately the sinusoidal components making up the first, third, and fifth harmonics of section 610 and section 612. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal 608 is shown as a square wave, there are

only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. 6H.

The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal 306 and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal 306. According to an embodiment of the invention, the input signal 606 may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

A filter 308 filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired harmonic frequency or frequencies as an output signal 310, shown for example as a filtered output signal 614 in FIG. 6I.

FIG. 4 illustrates an example universal frequency up-conversion (UFU) module 401. The UFU module 401 includes an example switch module 304, which comprises a bias signal 402, a resistor or impedance 404, a universal frequency translator (UFT) 450, and a ground 408. The UFT 450 includes a switch 406. The input signal 302 (designated as "Control Signal" in FIG. 4) controls the switch 406 in the UFT 450, and causes it to close and open. Harmonically rich signal 306 is generated at a node 405 located between the resistor or impedance 404 and the switch 406.

Also in FIG. 4, it can be seen that an example filter 308 is comprised of a capacitor 410 and an inductor 412 shunted to a ground 414. The filter is designed to filter out the undesired harmonics of harmonically rich signal 306.

The invention is not limited to the UFU embodiment shown in FIG. 4

For example, in an alternate embodiment shown in FIG. 5, an unshaped input signal 501 is routed to a pulse shaping module 502. The pulse shaping module 502 modifies the unshaped input signal 501 to generate a (modified) input signal 302 (designated as the "Control Signal" in FIG. 5). The input signal 302 is routed to the

switch module 304, which operates in the manner described above. Also, the filter 308 of FIG. 5 operates in the manner described above.

The purpose of the pulse shaping module 502 is to define the pulse width of the input signal 302. Recall that the input signal 302 controls the opening and closing of the switch 406 in switch module 304. During such operation, the pulse width of the input signal 302 establishes the pulse width of the harmonically rich signal 306. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal 306 are a function of at least the pulse width of the harmonically rich signal 306. As such, the pulse width of the input signal 302 contributes to setting the relative amplitudes of the harmonics of harmonically rich signal 306.

Further details of up-conversion as described in this section are presented in pending U.S. application "Method and System for Frequency Up-Conversion," Ser. No. 09/176,154, filed October 21, 1998, incorporated herein by reference in its entirety.

4.   *Enhanced Signal Reception*

The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same.

Referring to FIG. 21, transmitter 2104 accepts a modulating baseband signal 2102 and generates (transmitted) redundant spectrums 2106a-n, which are sent over communications medium 2108. Receiver 2112 recovers a demodulated baseband signal 2114 from (received) redundant spectrums 2110a-n. Demodulated baseband signal 2114 is representative of the modulating baseband signal 2102, where the level of similarity between the modulating baseband signal 2114 and the modulating baseband signal 2102 is application dependent.

Modulating baseband signal 2102 is preferably any information signal desired for transmission and/or reception. An example modulating baseband signal 2202 is

illustrated in FIG. 22A, and has an associated modulating baseband spectrum 2204 and image spectrum 2203 that are illustrated in FIG. 22B. Modulating baseband signal 2202 is illustrated as an analog signal in FIG. 22a, but could also be a digital signal, or combination thereof. Modulating baseband signal 2202 could be a voltage (or current) characterization of any number of real world occurrences, including for example and without limitation, the voltage (or current) representation for a voice signal.

Each transmitted redundant spectrum 2106a-n contains the necessary information to substantially reconstruct the modulating baseband signal 2102. In other words, each redundant spectrum 2106a-n contains the necessary amplitude, phase, and frequency information to reconstruct the modulating baseband signal 2102.

FIG. 22C illustrates example transmitted redundant spectrums 2206b-d. Transmitted redundant spectrums 2206b-d are illustrated to contain three redundant spectrums for illustration purposes only. Any number of redundant spectrums could be generated and transmitted as will be explained in following discussions.

Transmitted redundant spectrums 2206b-d are centered at f_1, with a frequency spacing f_2 between adjacent spectrums. Frequencies f_1 and f_2 are dynamically adjustable in real-time as will be shown below. FIG. 22D illustrates an alternate embodiment, where redundant spectrums 2208c,d are centered on unmodulated oscillating signal 2209 at f_1 (Hz). Oscillating signal 2209 may be suppressed if desired using, for example, phasing techniques or filtering techniques. Transmitted redundant spectrums are preferably above baseband frequencies as is represented by break 2205 in the frequency axis of FIGS. 22C and 22D.

Received redundant spectrums 2110a-n are substantially similar to transmitted redundant spectrums 2106a-n, except for the changes introduced by the communications medium 2108. Such changes can include but are not limited to signal attenuation, and signal interference. FIG. 22E illustrates example received redundant spectrums 2210b-d. Received redundant spectrums 2210b-d are substantially similar

to transmitted redundant spectrums 2206b-d, except that redundant spectrum 2210c includes an undesired jamming signal spectrum 2211 in order to illustrate some advantages of the present invention. Jamming signal spectrum 2211 is a frequency spectrum associated with a jamming signal. For purposes of this invention, a "jamming signal" refers to any unwanted signal, regardless of origin, that may interfere with the proper reception and reconstruction of an intended signal. Furthermore, the jamming signal is not limited to tones as depicted by spectrum 2211, and can have any spectral shape, as will be understood by those skilled in the art(s).

As stated above, demodulated baseband signal 2114 is extracted from one or more of received redundant spectrums 2210b-d. FIG. 22F illustrates example demodulated baseband signal 2212 that is, in this example, substantially similar to modulating baseband signal 2202 (FIG. 22A); where in practice, the degree of similarity is application dependent.

An advantage of the present invention should now be apparent. The recovery of modulating baseband signal 2202 can be accomplished by receiver 2112 in spite of the fact that high strength jamming signal(s) (e.g. jamming signal spectrum 2211) exist on the communications medium. The intended baseband signal can be recovered because multiple redundant spectrums are transmitted, where each redundant spectrum carries the necessary information to reconstruct the baseband signal. At the destination, the redundant spectrums are isolated from each other so that the baseband signal can be recovered even if one or more of the redundant spectrums are corrupted by a jamming signal.

Transmitter 2104 will now be explored in greater detail. FIG. 23A illustrates transmitter 2301, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2206b-d. Transmitter 2301 includes generator 2303, optional spectrum processing module 2304, and optional medium interface module 2320. Generator 2303 includes: first oscillator

2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

Transmitter 2301 operates as follows. First oscillator 2302 and second oscillator 2309 generate a first oscillating signal 2305 and second oscillating signal 2312, respectively. First stage modulator 2306 modulates first oscillating signal 2305 with modulating baseband signal 2202, resulting in modulated signal 2308. First stage modulator 2306 may implement any type of modulation including but not limited to: amplitude modulation, frequency modulation, phase modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates modulated signal 2308 with second oscillating signal 2312, resulting in multiple redundant spectrums 2206a-n shown in FIG. 23B. Second stage modulator 2310 is preferably a phase modulator, or a frequency modulator, although other types of modulation may be implemented including but not limited to amplitude modulation. Each redundant spectrum 2206a-n contains the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal 2202.

Redundant spectrums 2206a-n are substantially centered around f_1, which is the characteristic frequency of first oscillating signal 2305. Also, each redundant spectrum 2206a-n (except for 2206c) is offset from f_1 by approximately a multiple of f_2 (Hz), where f_2 is the frequency of the second oscillating signal 2312. Thus, each redundant spectrum 2206a-n is offset from an adjacent redundant spectrum by f_2 (Hz). This allows the spacing between adjacent redundant spectrums to be adjusted (or tuned) by changing f_2 that is associated with second oscillator 2309. Adjusting the spacing between adjacent redundant spectrums allows for dynamic real-time tuning of the bandwidth occupied by redundant spectrums 2206a-n.

In one embodiment, the number of redundant spectrums 2206a-n generated by transmitter 2301 is arbitrary and may be unlimited as indicated by the "a-n" designation for redundant spectrums 2206a-n. However, a typical communications

medium will have a physical and/or administrative limitations (i.e. FCC regulations) that restrict the number of redundant spectrums that can be practically transmitted over the communications medium. Also, there may be other reasons to limit the number of redundant spectrums transmitted. Therefore, preferably, the transmitter 2301 will include an optional spectrum processing module 2304 to process the redundant spectrums 2206a-n prior to transmission over communications medium 2108.

In one embodiment, spectrum processing module 2304 includes a filter with a passband 2207 (FIG. 23C) to select redundant spectrums 2206b-d for transmission. This will substantially limit the frequency bandwidth occupied by the redundant spectrums to the passband 2207. In one embodiment, spectrum processing module 2304 also up converts redundant spectrums and/or amplifies redundant spectrums prior to transmission over the communications medium 2108. Finally, medium interface module 2320 transmits redundant spectrums over the communications medium 2108. In one embodiment, communications medium 2108 is an over-the-air link and medium interface module 2320 is an antenna. Other embodiments for communications medium 2108 and medium interface module 2320 will be understood based on the teachings contained herein.

FIG. 23D illustrates transmitter 2321, which is one embodiment of transmitter 2104 that generates redundant spectrums configured similar to redundant spectrums 2208c-d and unmodulated spectrum 2209. Transmitter 2321 includes generator 2311, spectrum processing module 2304, and (optional) medium interface module 2320. Generator 2311 includes: first oscillator 2302, second oscillator 2309, first stage modulator 2306, and second stage modulator 2310.

As shown in FIG. 23D, many of the components in transmitter 2321 are similar to those in transmitter 2301. However, in this embodiment, modulating baseband signal 2202 modulates second oscillating signal 2312. Transmitter 2321 operates as follows. First stage modulator 2306 modulates second oscillating signal

2312 with modulating baseband signal 2202, resulting in modulated signal 2322. As described earlier, first stage modulator 2306 can effect any type of modulation including but not limited to: amplitude modulation frequency modulation, combinations thereof, or any other type of modulation. Second stage modulator 2310 modulates first oscillating signal 2304 with modulated signal 2322, resulting in redundant spectrums 2208a-n, as shown in FIG. 23E. Second stage modulator 2310 is preferably a phase or frequency modulator, although other modulators could used including but not limited to an amplitude modulator.

Redundant spectrums 2208a-n are centered on unmodulated spectrum 2209 (at f_1 Hz), and adjacent spectrums are separated by f_2 Hz. The number of redundant spectrums 2208a-n generated by generator 2311 is arbitrary and unlimited, similar to spectrums 2206a-n discussed above. Therefore, optional spectrum processing module 2304 may also include a filter with passband 2325 to select, for example, spectrums 2208c,d for transmission over communications medium 2108. In addition, optional spectrum processing module 2304 may also include a filter (such as a bandstop filter) to attenuate unmodulated spectrum 2209. Alternatively, unmodulated spectrum 2209 may be attenuated by using phasing techniques during redundant spectrum generation. Finally, (optional) medium interface module 2320 transmits redundant spectrums 2208c,d over communications medium 2108.

Receiver 2112 will now be explored in greater detail to illustrate recovery of a demodulated baseband signal from received redundant spectrums. FIG. 24A illustrates receiver 2430, which is one embodiment of receiver 2112. Receiver 2430 includes optional medium interface module 2402, down-converter 2404, spectrum isolation module 2408, and data extraction module 2414. Spectrum isolation module 2408 includes filters 2410a-c. Data extraction module 2414 includes demodulators 2416a-c, error check modules 2420a-c, and arbitration module 2424. Receiver 2430 will be discussed in relation to the signal diagrams in FIGS. 24B-24J.

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In one embodiment, optional medium interface module 2402 receives redundant spectrums 2210b-d (FIG. 22E, and FIG. 24B). Each redundant spectrum 2210b-d includes the necessary amplitude, phase, and frequency information to substantially reconstruct the modulating baseband signal used to generated the redundant spectrums. However, in the present example, spectrum 2210c also contains jamming signal 2211, which may interfere with the recovery of a baseband signal from spectrum 2210c. Down-converter 2404 down-converts received redundant spectrums 2210b-d to lower intermediate frequencies, resulting in redundant spectrums 2406a-c (FIG. 24C). Jamming signal 2211 is also down-converted to jamming signal 2407, as it is contained within redundant spectrum 2406b. Spectrum isolation module 2408 includes filters 2410a-c that isolate redundant spectrums 2406a-c from each other (FIGS. 24D-24F, respectively). Demodulators 2416a-c independently demodulate spectrums 2406a-c, resulting in demodulated baseband signals 2418a-c, respectively (FIGS. 24G-24I). Error check modules 2420a-c analyze demodulate baseband signal 2418a-c to detect any errors. In one embodiment, each error check module 2420a-c sets an error flag 2422a-c whenever an error is detected in a demodulated baseband signal. Arbitration module 2424 accepts the demodulated baseband signals and associated error flags, and selects a substantially error-free demodulated baseband signal (FIG. 24J). In one embodiment, the substantially error-free demodulated baseband signal will be substantially similar to the modulating baseband signal used to generate the received redundant spectrums, where the degree of similarity is application dependent.

Referring to FIGS. 24G-I, arbitration module 2424 will select either demodulated baseband signal 2418a or 2418c, because error check module 2420b will set the error flag 2422b that is associated with demodulated baseband signal 2418b.

The error detection schemes implemented by the error detection modules include but are not limited to: cyclic redundancy check (CRC) and parity check for digital signals, and various error detections schemes for analog signal.

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Further details of enhanced signal reception as described in this section are presented in pending U.S. application "Method and System for Ensuring Reception of a Communications Signal," Ser. No. 09/176,415, filed October 21, 1998, incorporated herein by reference in its entirety.

5

5. Unified Down-conversion and Filtering

The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

10   In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at 15 substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

FIG. 17 is a conceptual block diagram of a UDF module 1702 according to 20 an embodiment of the present invention. The UDF module 1702 performs at least frequency translation and frequency selectivity.

The effect achieved by the UDF module 1702 is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module 1702 effectively performs input filtering.

25   According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited

to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

In embodiments of the invention, input signals 1704 received by the UDF module 1702 are at radio frequencies. The UDF module 1702 effectively operates to input filter these RF input signals 1704. Specifically, in these embodiments, the UDF module 1702 effectively performs input, channel select filtering of the RF input signal 1704. Accordingly, the invention achieves high selectivity at high frequencies.

The UDF module 1702 effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

Conceptually, the UDF module 1702 includes a frequency translator 1708. The frequency translator 1708 conceptually represents that portion of the UDF module 1702 that performs frequency translation (down conversion).

The UDF module 1702 also conceptually includes an apparent input filter 1706 (also sometimes called an input filtering emulator). Conceptually, the apparent input filter 1706 represents that portion of the UDF module 1702 that performs input filtering.

In practice, the input filtering operation performed by the UDF module 1702 is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter 1706 is herein referred to as an "apparent" input filter 1706.

The UDF module 1702 of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module 1702. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module 1702 can be designed with a filter center frequency f_C on the order of 900 MHZ, and a filter

bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as discussed herein is not applicable.

The invention exhibits additional advantages. For example, the filtering center frequency f_c of the UDF module 1702 can be electrically adjusted, either statically or dynamically.

Also, the UDF module 1702 can be designed to amplify input signals.

Further, the UDF module 1702 can be implemented without large resistors, capacitors, or inductors. Also, the UDF module 1702 does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module 1702 is friendly to integrated circuit design techniques and processes.

The features and advantages exhibited by the UDF module 1702 are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF module 1702 performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to frequency translation also contribute to the performance of frequency selectivity, and vice versa.

According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and samples/instances of the output signal.

More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

Next, the input sample is held (that is, delayed).

Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module preferably performs input filtering and frequency down-conversion in a unified manner.

FIG. 19 illustrates an example implementation of the unified down-converting and filtering (UDF) module 1922. The UDF module 1922 performs the frequency translation operation and the frequency selectivity operation in an integrated, unified manner as described above, and as further described below.

In the example of FIG. 19, the frequency selectivity operation performed by the UDF module 1922 comprises a band-pass filtering operation according to EQ. 1, below, which is an example representation of a band-pass filtering transfer function.

$$VO = \alpha_1 \, z^{-1} VI - \beta_1 \, z^{-1} VO - \beta_0 \, z^{-2} VO \qquad \text{EQ. 1}$$

It should be noted, however, that the invention is not limited to band-pass filtering. Instead, the invention effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof. As will be appreciated, there are many representations of any given filter type. The

1744 0450003

invention is applicable to these filter representations. Thus, EQ. 1 is referred to herein for illustrative purposes only, and is not limiting.

The UDF module 1922 includes a down-convert and delay module 1924, first and second delay modules 1928 and 1930, first and second scaling modules 1932 and 1934, an output sample and hold module 1936, and an (optional) output smoothing module 1938. Other embodiments of the UDF module will have these components in different configurations, and/or a subset of these components, and/or additional components. For example, and without limitation, in the configuration shown in FIG. 19, the output smoothing module 1938 is optional.

As further described below, in the example of FIG. 19, the down-convert and delay module 1924 and the first and second delay modules 1928 and 1930 include switches that are controlled by a clock having two phases, ϕ_1 and ϕ_2. ϕ_1 and ϕ_2 preferably have the same frequency, and are non-overlapping (alternatively, a plurality such as two clock signals having these characteristics could be used). As used herein, the term "non-overlapping" is defined as two or more signals where only one of the signals is active at any given time. In some embodiments, signals are "active" when they are high. In other embodiments, signals are active when they are low.

Preferably, each of these switches closes on a rising edge of ϕ_1 or ϕ_2, and opens on the next corresponding falling edge of ϕ_1 or ϕ_2. However, the invention is not limited to this example. As will be apparent to persons skilled in the relevant art(s), other clock conventions can be used to control the switches.

In the example of FIG. 19, it is assumed that α_1 is equal to one. Thus, the output of the down-convert and delay module 1924 is not scaled. As evident from the embodiments described above, however, the invention is not limited to this example.

The example UDF module 1922 has a filter center frequency of 900.2 MHZ and a filter bandwidth of 570 KHz. The pass band of the UDF module 1922 is on the

order of 899.915 MHZ to 900.485 MHZ. The Q factor of the UDF module 1922 is approximately 1879 (i.e., 900.2 MHZ divided by 570 KHz).

The operation of the UDF module 1922 shall now be described with reference to a Table 1802 (FIG. 18) that indicates example values at nodes in the UDF module 1922 at a number of consecutive time increments. It is assumed in Table 1802 that the UDF module 1922 begins operating at time t-1. As indicated below, the UDF module 1922 reaches steady state a few time units after operation begins. The number of time units necessary for a given UDF module to reach steady state depends on the configuration of the UDF module, and will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

At the rising edge of ϕ_1 at time t-1, a switch 1950 in the down-convert and delay module 1924 closes. This allows a capacitor 1952 to charge to the current value of an input signal, VI_{t-1}, such that node 1902 is at VI_{t-1}. This is indicated by cell 1804 in FIG. 18. In effect, the combination of the switch 1950 and the capacitor 1952 in the down-convert and delay module 1924 operates to translate the frequency of the input signal VI to a desired lower frequency, such as IF or baseband. Thus, the value stored in the capacitor 1952 represents an instance of a down-converted image of the input signal VI.

The manner in which the down-convert and delay module 1924 performs frequency down-conversion is further described elsewhere in this application, and is additionally described in pending U.S. application "Method and System for Down-Converting Electromagnetic Signals," Ser. No. 09/176,022, filed October 21, 1998, which is herein incorporated by reference in its entirety.

Also at the rising edge of ϕ_1 at time t-1, a switch 1958 in the first delay module 1928 closes, allowing a capacitor 1960 to charge to VO_{t-1}, such that node 1906 is at VO_{t-1}. This is indicated by cell 1806 in Table 1802. (In practice, VO_{t-1} is undefined at this point. However, for ease of understanding, VO_{t-1} shall continue to be used for purposes of explanation.)

1744 0450003

Also at the rising edge of ϕ_1 at time t-1, a switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to a value stored in a capacitor 1964. At this time, however, the value in capacitor 1964 is undefined, so the value in capacitor 1968 is undefined. This is indicated by cell 1807 in table 1802.

At the rising edge of ϕ_2 at time t-1, a switch 1954 in the down-convert and delay module 1924 closes, allowing a capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_{t-1}, such that node 1904 is at VI_{t-1}. This is indicated by cell 1810 in Table 1802.

The UDF module 1922 may optionally include a unity gain module 1990A between capacitors 1952 and 1956. The unity gain module 1990A operates as a current source to enable capacitor 1956 to charge without draining the charge from capacitor 1952. For a similar reason, the UDF module 1922 may include other unity gain modules 1990B-1990G. It should be understood that, for many embodiments and applications of the invention, these unity gain modules 1990A-1990G are optional. The structure and operation of the unity gain modules 1990 will be apparent to persons skilled in the relevant art(s).

Also at the rising edge of ϕ_2 at time t-1, a switch 1962 in the first delay module 1928 closes, allowing a capacitor 1964 to charge to the level of the capacitor 1960. Accordingly, the capacitor 1964 charges to VO_{t-1}, such that node 1908 is at VO_{t-1}. This is indicated by cell 1814 in Table 1802.

Also at the rising edge of ϕ_2 at time t-1, a switch 1970 in the second delay module 1930 closes, allowing a capacitor 1972 to charge to a value stored in a capacitor 1968. At this time, however, the value in capacitor 1968 is undefined, so the value in capacitor 1972 is undefined. This is indicated by cell 1815 in table 1802.

At time t, at the rising edge of ϕ_1, the switch 1950 in the down-convert and delay module 1924 closes. This allows the capacitor 1952 to charge to VI_t, such that node 1902 is at VI_t. This is indicated in cell 1816 of Table 1802.

Also at the rising edge of ϕ_1 at time t, the switch 1958 in the first delay module 1928 closes, thereby allowing the capacitor 1960 to charge to VO_t. Accordingly, node 1906 is at VO_t. This is indicated in cell 1820 in Table 1802.

Further at the rising edge of ϕ_1 at time t, the switch 1966 in the second delay module 1930 closes, allowing a capacitor 1968 to charge to the level of the capacitor 1964. Therefore, the capacitor 1968 charges to VO_{t-1}, such that node 1910 is at VO_{t-1}. This is indicated by cell 1824 in Table 1802.

At the rising edge of ϕ_2 at time t, the switch 1954 in the down-convert and delay module 1924 closes, allowing the capacitor 1956 to charge to the level of the capacitor 1952. Accordingly, the capacitor 1956 charges to VI_t, such that node 1904 is at VI_t. This is indicated by cell 1828 in Table 1802

Also at the rising edge of ϕ_2 at time t, the switch 1962 in the first delay module 1928 closes, allowing the capacitor 1964 to charge to the level in the capacitor 1960. Therefore, the capacitor 1964 charges to VO_t, such that node 1908 is at VO_t. This is indicated by cell 1832 in Table 1802.

Further at the rising edge of ϕ_2 at time t, the switch 1970 in the second delay module 1930 closes, allowing the capacitor 1972 in the second delay module 1930 to charge to the level of the capacitor 1968 in the second delay module 1930. Therefore, the capacitor 1972 charges to VO_{t-1}, such that node 1912 is at VO_{t-1}. This is indicated in cell 1836 of FIG. 18.

At time t+1, at the rising edge of ϕ_1, the switch 1950 in the down-convert and delay module 1924 closes, allowing the capacitor 1952 to charge to VI_{t+1}. Therefore, node 1902 is at VI_{t+1}, as indicated by cell 1838 of Table 1802.

Also at the rising edge of ϕ_1 at time t+1, the switch 1958 in the first delay module 1928 closes, allowing the capacitor 1960 to charge to VO_{t+1}. Accordingly, node 1906 is at VO_{t+1}, as indicated by cell 1842 in Table 1802.

Further at the rising edge of ϕ_1 at time t+1, the switch 1966 in the second delay module 1930 closes, allowing the capacitor 1968 to charge to the level of the

capacitor 1964. Accordingly, the capacitor 1968 charges to VO_t, as indicated by cell 1846 of Table 1802.

In the example of FIG. 19, the first scaling module 1932 scales the value at node 1908 (i.e., the output of the first delay module 1928) by a scaling factor of -0.1. Accordingly, the value present at node 1914 at time t+1 is -0.1 $*$ VO_t. Similarly, the second scaling module 1934 scales the value present at node 1912 (i.e., the output of the second scaling module 1930) by a scaling factor of -0.8. Accordingly, the value present at node 1916 is -0.8 $*$ VO_{t-1} at time t+1.

At time t+1, the values at the inputs of the summer 1926 are: VI_t at node 1904, -0.1 $*$ VO_t at node 1914, and -0.8 $*$ VO_{t-1} at node 1916 (in the example of FIG. 19, the values at nodes 1914 and 1916 are summed by a second summer 1925, and this sum is presented to the summer 1926). Accordingly, at time t+1, the summer generates a signal equal to VI_t - 0.1 $*$ VO_t - 0.8 $*$ VO_{t-1}.

At the rising edge of ϕ_1 at time t+1, a switch 1991 in the output sample and hold module 1936 closes, thereby allowing a capacitor 1992 to charge to VO_{t+1} Accordingly, the capacitor 1992 charges to VO_{t+1}, which is equal to the sum generated by the adder 1926. As just noted, this value is equal to: VI_t - 0.1 $*$ VO_t - 0.8 $*$ VO_{t-1}. This is indicated in cell 1850 of Table 1802. This value is presented to the optional output smoothing module 1938, which smooths the signal to thereby generate the instance of the output signal VO_{t+1}. It is apparent from inspection that this value of VO_{t+1} is consistent with the band pass filter transfer function of EQ. 1.

Further details of unified down-conversion and filtering as described in this section are presented in pending U.S. application "Integrated Frequency Translation And Selectivity," Ser. No. 09/175,966, filed October 21, 1998, incorporated herein by reference in its entirety.

6. *Example Application Embodiments of the Invention*

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As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

Example applications of the UFT module were described above. In particular, frequency down-conversion, frequency up-conversion, enhanced signal reception, and unified down-conversion and filtering applications of the UFT module were summarized above, and are further described below. These applications of the UFT module are discussed herein for illustrative purposes. The invention is not limited to these example applications. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s), based on the teachings contained herein.

For example, the present invention can be used in applications that involve frequency down-conversion. This is shown in FIG. 1C, for example, where an example UFT module 115 is used in a down-conversion module 114. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal This is also shown in FIG. 7, for example, where an example UFT module 706 is part of a down-conversion module 704, which is part of a receiver 702.

The present invention can be used in applications that involve frequency up-conversion. This is shown in FIG. 1D, for example, where an example UFT module 117 is used in a frequency up-conversion module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal. This is also shown in FIG. 8, for example, where an example UFT module 806 is part of up-conversion module 804, which is part of a transmitter 802.

The present invention can be used in environments having one or more transmitters 902 and one or more receivers 906, as illustrated in FIG. 9. In such environments, one or more of the transmitters 902 may be implemented using a UFT

module, as shown for example in FIG. 8. Also, one or more of the receivers 906 may be implemented using a UFT module, as shown for example in FIG. 7.

The invention can be used to implement a transceiver. An example transceiver 1002 is illustrated in FIG. 10. The transceiver 1002 includes a transmitter 1004 and a receiver 1008. Either the transmitter 1004 or the receiver 1008 can be implemented using a UFT module. Alternatively, the transmitter 1004 can be implemented using a UFT module 1006, and the receiver 1008 can be implemented using a UFT module 1010. This embodiment is shown in FIG. 10.

Another transceiver embodiment according to the invention is shown in FIG. 11. In this transceiver 1102, the transmitter 1104 and the receiver 1108 are implemented using a single UFT module 1106. In other words, the transmitter 1104 and the receiver 1108 share a UFT module 1106.

As described elsewhere in this application, the invention is directed to methods and systems for enhanced signal reception (ESR). Various ESR embodiments include an ESR module (transmit) in a transmitter 1202, and an ESR module (receive) in a receiver 1210. An example ESR embodiment configured in this manner is illustrated in FIG. 12.

The ESR module (transmit) 1204 includes a frequency up-conversion module 1206. Some embodiments of this frequency up-conversion module 1206 may be implemented using a UFT module, such as that shown in FIG. 1D.

The ESR module (receive) 1212 includes a frequency down-conversion module 1214. Some embodiments of this frequency down-conversion module 1214 may be implemented using a UFT module, such as that shown in FIG. 1C.

As described elsewhere in this application, the invention is directed to methods and systems for unified down-conversion and filtering (UDF). An example unified down-conversion and filtering module 1302 is illustrated in FIG. 13. The unified down-conversion and filtering module 1302 includes a frequency down-conversion module 1304 and a filtering module 1306. According to the invention, the frequency

down-conversion module 1304 and the filtering module 1306 are implemented using a UFT module 1308, as indicated in FIG. 13.

Unified down-conversion and filtering according to the invention is useful in applications involving filtering and/or frequency down-conversion. This is depicted, for example, in FIGS. 15A-15F. FIGS. 15A-15C indicate that unified down-conversion and filtering according to the invention is useful in applications where filtering precedes, follows, or both precedes and follows frequency down-conversion. FIG. 15D indicates that a unified down-conversion and filtering module 1524 according to the invention can be utilized as a filter 1522 (i.e., where the extent of frequency down-conversion by the down-converter in the unified down-conversion and filtering module 1524 is minimized). FIG. 15E indicates that a unified down-conversion and filtering module 1528 according to the invention can be utilized as a down-converter 1526 (i.e., where the filter in the unified down-conversion and filtering module 1528 passes substantially all frequencies). FIG. 15F illustrates that the unified down-conversion and filtering module 1532 can be used as an amplifier. It is noted that one or more UDF modules can be used in applications that involve at least one or more of filtering, frequency translation, and amplification.

For example, receivers, which typically perform filtering, down-conversion, and filtering operations, can be implemented using one or more unified down-conversion and filtering modules. This is illustrated, for example, in FIG. 14.

The methods and systems of unified down-conversion and filtering of the invention have many other applications. For example, as discussed herein, the enhanced signal reception (ESR) module (receive) operates to down-convert a signal containing a plurality of spectrums. The ESR module (receive) also operates to isolate the spectrums in the down-converted signal, where such isolation is implemented via filtering in some embodiments. According to embodiments of the invention, the ESR module (receive) is implemented using one or more unified down-conversion and filtering (UDF) modules. This is illustrated, for example, in FIG. 16.

In the example of FIG. 16, one or more of the UDF modules 1610, 1612, 1614 operates to down-convert a received signal. The UDF modules 1610, 1612, 1614 also operate to filter the down-converted signal so as to isolate the spectrum(s) contained therein. As noted above, the UDF modules 1610, 1612, 1614 are implemented using the universal frequency translation (UFT) modules of the invention.

The invention is not limited to the applications of the UFT module described above. For example, and without limitation, subsets of the applications (methods and/or structures) described herein (and others that would be apparent to persons skilled in the relevant art(s) based on the herein teachings) can be associated to form useful combinations.

For example, transmitters and receivers are two applications of the UFT module. FIG. 10 illustrates a transceiver 1002 that is formed by combining these two applications of the UFT module, i.e., by combining a transmitter 1004 with a receiver 1008.

Also, ESR (enhanced signal reception) and unified down-conversion and filtering are two other applications of the UFT module. FIG. 16 illustrates an example where ESR and unified down-conversion and filtering are combined to form a modified enhanced signal reception system.

The invention is not limited to the example applications of the UFT module discussed herein. Also, the invention is not limited to the example combinations of applications of the UFT module discussed herein. These examples were provided for illustrative purposes only, and are not limiting. Other applications and combinations of such applications will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion; (4) receiving; (5) transmitting; (6) filtering; and/or (7)

signal transmission and reception in environments containing potentially jamming signals.

Additional example applications are described below.

5   ## 7.   *Universal Transmitter*

The present invention is directed at a universal transmitter using, in embodiments, two or more UFT modules in a balanced vector modulator configuration. The universal transmitter can be used to create virtually every known

10   and useful waveform used in analog and digital communications applications in wired and wireless markets. By appropriately selecting the inputs to the universal transmitter, a host of signals can be synthesized including but not limited to AM, FM, BPSK, QPSK, MSK, QAM, ODFM, multi-tone, and spread-spectrum signals (including CDMA and frequency hopping). As will be shown, the universal transmitter

15   can up-convert these waveforms using less components than that seen with conventional super-hetrodyne approaches. In other words, the universal transmitter does not require multiple IF stages (having intermediate filtering) to up-convert complex waveforms that have demanding spectral growth requirements. The elimination of intermediate IF stages reduces part count in the transmitter and

20   therefore leads to cost savings. As will be shown, the present invention achieves these savings without sacrificing performance.

Furthermore, the use of a balanced configuration means that carrier insertion can be attenuated or controlled during up-conversion of a baseband signal. Carrier insertion is caused by the variation of transmitter components (e.g. resistors,

25   capacitors, etc.), which produces DC offset voltages throughout the transmitter. Any DC offset voltage gets up-converted, along with the baseband signal, and generates spectral energy (or carrier insertion) at the carrier frequency f_c. In many transmit applications, it is highly desirable to minimize the carrier insertion in an up-converted

1744.0450003

signal because the sideband(s) carry the baseband information and any carrier insertion is wasted energy that reduces efficiency.

FIGs. 25A-B graphically illustrate carrier insertion in the context of up-converted signals that carry baseband information in the corresponding signal sidebands. FIG. 25A depicts an up-converted signal 2502 having minimal carrier energy 2504 when compared to sidebands 2506a and 2506b. In these transmitter applications, the present invention can be configured to minimize carrier insertion by limiting the relative DC offset voltage that is present in the transmitter. Alternatively, some transmit applications require sufficient carrier insertion for coherent demodulation of the transmitted signal at the receiver. This illustrated by FIG. 25B, which shows up-converted signal 2508 having carrier energy 2510 that is somewhat larger than sidebands 2512a and 2512b. In these applications, the present invention can be configured to introduce a DC offset voltage that generates the desired carrier insertion.

7.1 Universal Transmitter Having 2 UFT Modules

FIG. 26A illustrates a transmitter 2602 according to embodiments of the present invention. Transmitter 2602 includes a balanced modulator/up-converter 2604, a control signal generator 2642, an optional filter 2606, and an optional amplifier 2608. Transmitter 2602 up-converts a baseband signal 2610 to produce an output signal 2640 that is conditioned for wireless or wire line transmission. In doing so, the balanced modulator 2604 receives the baseband signal 2610 and samples the baseband signal in a differential and balanced fashion to generate a harmonically rich signal 2638. The harmonically rich signal 2638 includes multiple harmonic images, where each image contains the baseband information in the baseband signal 2610. The optional bandpass filter 2606 may be included to select a harmonic of interest (or a subset of harmonics) in the signal 2558 for transmission. The optional amplifier 2608

may be included to amplify the selected harmonic prior to transmission. The universal transmitter is further described at a high level by the flowchart 6200 that is shown in FIG. 62. A more detailed structural and operational description of the balanced modulator follows thereafter.

Referring to flowchart 6200, in step 6202, the balanced modulator 2604 receives the baseband signal 2610.

In step 6204, the balanced modulator 2604 samples the baseband signal in a differential and balanced fashion according to a first and second control signals that are phase shifted with respect to each other. The resulting harmonically rich signal 2638 includes multiple harmonic images that repeat at harmonics of the sampling frequency, where each image contains the necessary amplitude and frequency information to reconstruct the baseband signal 2610.

In embodiments of the invention, the control signals include pulses having pulse widths (or apertures) that are established to improve energy transfer to a desired harmonic of the harmonically rich signal. In further embodiments of the invention, DC offset voltages are minimized between sampling modules as indicated in step 6206, thereby minimizing carrier insertion in the harmonic images of the harmonically rich signal 2638.

In step 6208, the optional bandpass filter 2606 selects the desired harmonic of interest (or a subset of harmonics) in from the harmonically rich signal 2638 for transmission.

In step 6210, the optional amplifier 2608 amplifies the selected harmonic(s) prior to transmission.

In step 6212, the selected harmonic(s) is transmitted over a communications medium.

7.1.1   Balanced Modulator Detailed Description

Referring to the example embodiment shown in FIG. 26A, the balanced modulator 2604 includes the following components: a buffer/inverter 2612; summer amplifiers 2618, 2619; UFT modules 2624 and 2628 having controlled switches 2648 and 2650, respectively; an inductor 2626; a blocking capacitor 2636; and a DC terminal 2611. As stated above, the balanced modulator 2604 differentially samples the baseband signal 2610 to generate a harmonically rich signal 2638. More specifically, the UFT modules 2624 and 2628 sample the baseband signal in differential fashion according to control signals 2623 and 2627, respectively. A DC reference voltage 2613 is applied to terminal 2611 and is uniformly distributed to the UFT modules 2624 and 2628. The distributed DC voltage 2613 prevents any DC offset voltages from developing between the UFT modules, which can lead to carrier insertion in the harmonically rich signal 2638 as described above. The operation of the balanced modulator 2604 is discussed in greater detail with reference to flowchart 6300 (FIG. 63), as follows.

In step 6302, the buffer/inverter 2612 receives the input baseband signal 2610 and generates input signal 2614 and inverted input signal 2616. Input signal 2614 is substantially similar to signal 2610, and inverted signal 2616 is an inverted version of signal 2614. As such, the buffer/inverter 2612 converts the (single-ended) baseband signal 2610 into differential input signals 2614 and 2616 that will be sampled by the UFT modules. Buffer/inverter 2612 can be implemented using known operational amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step 6304, the summer amplifier 2618 sums the DC reference voltage 2613 applied to terminal 2611 with the input signal 2614, to generate a combined signal 2620. Likewise, the summer amplifier 2619 sums the DC reference voltage 2613 with the inverted input signal 2616 to generate a combined signal 2622. Summer amplifiers 2618 and 2619 can be implemented using known op amp summer circuits, and can be designed to have a specified gain or attenuation, including unity gain, although the

invention is not limited to this example. The DC reference voltage 2613 is also distributed to the outputs of both UFT modules 2624 and 2628 through the inductor 2626 as is shown.

In step 6306, the control signal generator 2642 generates control signals 2623 and 2627 that are shown by way of example in FIG. 27B and FIG. 27C, respectively. As illustrated, both control signals 2623 and 2627 have the same period T_S as a master clock signal 2645 (FIG.27A), but have a pulse width (or aperture) of T_A. In the example, control signal 2623 triggers on the rising pulse edge of the master clock signal 2645, and control signal 2627 triggers on the falling pulse edge of the master clock signal 2645. Therefore, control signals 2623 and 2627 are shifted in time by 180 degrees relative to each other. In embodiments of invention, the master clock signal 2645 (and therefore the control signals 2623 and 2627) have a frequency that is a subharmonic of the desired output signal 2640. The invention is not limited to the example of FIGs. 27A-27C.

In one embodiment, the control signal generator 2642 includes an oscillator 2646, pulse generators 2644a and 2644b, and an inverter 2647 as shown. In operation, the oscillator 2646 generates the master clock signal 2645, which is illustrated in FIG. 27A as a periodic square wave having pulses with a period of T_S. Other clock signals could be used including but not limited to sinusoidal waves, as will be understood by those skilled in the arts. Pulse generator 2644a receives the master clock signal 2645 and triggers on the rising pulse edge, to generate the control signal 2623. Inverter 2647 inverts the clock signal 2645 to generate an inverted clock signal 2643. The pulse generator 2644b receives the inverted clock signal 2643 and triggers on the rising pulse edge (which is the falling edge of clock signal 2645), to generate the control signal 2627.

FIG 74A-E illustrate example embodiments for the pulse generator 2644. FIG. 74A illustrates a pulse generator 7402. The pulse generator 7402 generates pulses 7408 having pulse width T_A from an input signal 7404. Example input signals 7404

1744.0450003

and pulses 7408 are depicted in FIGs 74B and 74C, respectively. The input signal 7404 can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave etc. The pulse width (or aperture) T_A of the pulses 7408 is determined by delay 7406 of the pulse generator 7402. The pulse generator 7402 also includes an optional inverter 7410, which is optionally added for polarity considerations as understood by those skilled in the arts. The example logic and implementation shown for the pulse generator 7402 is provided for illustrative purposes only, and is not limiting. The actual logic employed can take many forms. Additional examples of pulse generation logic are shown in FIGs. 74D and 74E. FIG. 74D illustrates a rising edge pulse generator 7412 that triggers on the rising edge of input signal 7404. FIG. 74E illustrates a falling edge pulse generator 7416 that triggers on the falling edge of the input signal 7404.

In step 6308, the UFT module 2624 samples the combined signal 2620 according to the control signal 2623 to generate harmonically rich signal 2630. More specifically, the switch 2648 closes during the pulse widths T_A of the control signal 2623 to sample the combined signal 2620 resulting in the harmonically rich signal 2630. FIG. 26B illustrates an exemplary frequency spectrum for the harmonically rich signal 2630 having harmonic images 2652a-n. The images 2652 repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image 2652 contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 2610. As discussed further below, the relative amplitude of the frequency images is generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic 2652 can be increased (or decreased) by adjusting the pulse width T_A of the control signal 2623. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled,

1744.0450003

"Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGs. 3-6. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in the co-pending patent application titled, "Method and System for Frequency Up-Conversion," Ser. No./09/176,154, field on October 21, 1998, and incorporated herein by reference.

In step 6310, the UFT module 2628 samples the combined signal 2622 according to the control signal 2627 to generate harmonically rich signal 2634. More specifically, the switch 2650 closes during the pulse widths T_A of the control signal 2627 to sample the combined signal 2622 resulting in the harmonically rich signal 2634. The harmonically rich signal 2634 includes multiple frequency images of baseband signal 2610 that repeat at harmonics of the sampling frequency $(1/T_s)$, similar to that for the harmonically rich signal 2630. However, the images in the signal 2634 are phase-shifted compared to those in signal 2630 because of the inversion of signal 2616 compared to signal 2614, and because of the relative phase shift between the control signals 2623 and 2627.

In step 6312, the node 2632 sums the harmonically rich signals 2632 and 2634 to generate harmonically rich signal 2633. FIG. 26C illustrates an exemplary frequency spectrum for the harmonically rich signal 2633 that has multiple images 2654a-n that repeat at harmonics of the sampling frequency $1/T_s$. Each image 2654 includes the necessary amplitude, frequency and phase information to reconstruct the baseband signal 2610. The capacitor 2636 operates as a DC blocking capacitor and substantially passes the harmonics in the harmonically rich signal 2633 to generate harmonically rich signal 2638 at the output of the modulator 2604.

In step 6208, the optional filter 2606 can be used to select a desired harmonic image for transmission. This is represented for example by a passband 2656 that selects the harmonic image 2654c for transmission in FIG. 26C.

An advantage of the modulator 2604 is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT

1744 0450003

modules 2624 and 2628. DC offset is minimized because the reference voltage 2613 contributes a consistent DC component to the input signals 2620 and 2622 through the summing amplifiers 2618 and 2619, respectively. Furthermore, the reference voltage 2613 is also directly coupled to the outputs of the UFT modules 2624 and 2628 through the inductor 2626 and the node 2632. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal 2638. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

7.1.2 Balanced Modulator Example Signal Diagrams and Mathematical Description

In order to further describe the invention, FIGs.27D-27I illustrate various example signal diagrams (vs. time) that are representative of the invention. These signal diagrams are meant for example purposes only and are not meant to be limiting. FIG. 27D illustrates a signal 2702 that is representative of the input baseband signal 2610 (FIG. 26A). FIG. 27E illustrates a step function 2704 that is an expanded portion of the signal 2702 from time t_0 to t_1, and represents signal 2614 at the output of the buffer/inverter 2612. Similarly, FIG. 27F illustrates a signal 2706 that is an inverted version of the signal 2704, and represents the signal 2616 at the inverted output of buffer/inverter 2612. For analysis purposes, a step function is a good approximation for a portion of a single bit of data (for the baseband signal 2610) because the clock rates of the control signals 2623 and 2627 are significantly higher than the data rates of the baseband signal 2610. For example, if the data rate is in the

KHz frequency range, then the clock rate will preferably be in MHZ frequency range in order to generate an output signal in the Ghz frequency range.

Still referring to FIGs. 27D-I, FIG. 27G illustrates a signal 2708 that an example of the harmonically rich signal 2630 when the step function 2704 is sampled according to the control signal 2623 in FIG. 27B. The signal 2708 includes positive pulses 2709 as referenced to the DC voltage 2613. Likewise, FIG. 27H illustrates a signal 2710 that is an example of the harmonically rich signal 2634 when the step function 2706 is sampled according to the control signal 2627. The signal 2710 includes negative pulses 2711 as referenced to the DC voltage 2613, which are time-shifted relative the positive pulses 2709 in signal 2708.

Still referring to FIGs. 27D-I, the FIG. 27I illustrates a signal 2712 that is the combination of signal 2708 (FIG. 27G) and the signal 2710 (FIG. 27H), and is an example of the harmonically rich signal 2633 at the output of the summing node 2632. As illustrated, the signal 2712 spends approximately as much time above the DC reference voltage 2613 as below the DC reference voltage 2613 over a limited time period. For example, over a time period 2714, the energy in the positive pulses 2709a-b is canceled out by the energy in the negative pulses 2711a-b. This is indicative of minimal (or zero) DC offset between the UFT modules 2624 and 2628, which results in minimal carrier insertion during the sampling process.

Still referring to FIG. 27I, the time axis of the signal 2712 can be phased in such a manner to represent the waveform as an odd function. For such an arrangement, the Fourier series is readily calculated to obtain:

$$I_c(t) = \sum_{n=1}^{\infty} \left(\frac{4\sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right) \cdot \sin\left(\frac{2n\pi t}{T_s}\right) \quad \textit{Equation 1.}$$

where: T_S = period of the master clock 2645

T_A = pulse width of the control signals 2623 and 2627

n= harmonic number

As shown by Equation 1, the relative amplitude of the frequency images is generally a function of the harmonic number n, and the ratio of T_A/T_S. As indicated, the T_A/T_S ratio represents the ratio of the pulse width of the control signals relative to the period of the sub-harmonic master clock. The T_A/T_S ratio can be optimized in order to maximize the amplitude of the frequency image at a given harmonic. For example, if a passband waveform is desired to be created at 5x the frequency of the sub-harmonic clock, then a baseline power for that harmonic extraction may be calculated for the fifth harmonic (n=5) as:

$$I_c(t) = \left(\frac{4 \sin\left(\frac{5\pi T_A}{T_s} \right)}{5\pi} \right) \cdot \sin(5\omega_s t) \qquad \textbf{\textit{Equation 2.}}$$

As shown by Equation 2, $I_C(t)$ for the fifth harmonic is a sinusoidal function having an amplitude that is proportional to the sin $(5\pi T_A/T_S)$. The signal amplitude can be maximized by setting $T_A = (1/10 \cdot T_S)$ so that sin $(5\pi T_A/T_S)$= sin $(\pi/2)$= 1. Doing so results in the equation:

$$I_c(t)\big|_{n=5} = \frac{4}{5\pi}\left(\sin\left(5\omega_s t\right)\right) \qquad \textbf{\textit{Equation 3.}}$$

1744.0450003

This component is a frequency at 5x of the sampling frequency of sub-harmonic clock, and can be extracted from the Fourier series via a bandpass filter (such as bandpass filter 2606) that is centered around $5f_S$. The extracted frequency component can then be optionally amplified by the amplifier 2608 prior to transmission on a wireless or wire-line communications channel or channels.

Equation 3 can be extended to reflect the inclusion of a message signal as illustrated by equation 4 below:

$$m(t) \cdot I_c(t) \Big|_{\substack{n=5 \\ \theta=\theta(t)}} = \frac{4 \cdot m(t)}{5\pi} \left(\sin\left(5\omega_s t + 5\theta(t)\right) \right) \qquad \textit{Equation 4.}$$

Equation 4 illustrates that a message signal can be carried in harmonically rich signals 2633 such that both amplitude and phase can be modulated. In other words, m(t) is modulated for amplitude and $\theta(t)$ is modulated for phase. In such cases, it should be noted that $\theta(t)$ is augmented modulo n while the amplitude modulation *m(t)* is simply scaled. Therefore, complex waveforms may be reconstructed from their Fourier series with multiple aperture UFT combinations.

As discussed above, the signal amplitude for the 5th harmonic was maximized by setting the sampling aperture width $T_A = 1/10 \ T_S$, where T_S is the period of the master clock signal. This can be restated and generalized as setting $T_A = \frac{1}{2}$ the period (or π radians) at the harmonic of interest. In other words, the signal amplitude of any harmonic n can be maximized by sampling the input waveform with a sampling aperture of $T_A = \frac{1}{2}$ the period of the harmonic of interest (n). Based on this discussion, it is apparent that varying the aperture changes the harmonic and amplitude content of the output waveform. For example, if the sub-harmonic clock has a frequency of 200 MHZ, then the fifth harmonic is at 1Ghz. The amplitude of the fifth harmonic is maximized by setting the aperture width $T_A = 500$ picoseconds, which equates to $\frac{1}{2}$ the period (or π radians) at 1 Ghz.

- 57 -

FIG. 27J depicts a frequency plot 2716 that graphically illustrates the effect of varying the sampling aperture of the control signals on the harmonically rich signal 2633 given a 200 MHZ harmonic clock. The frequency plot 2716 compares two frequency spectrums 2718 and 2720 for different control signal apertures given a 200 MHZ clock. More specifically, the frequency spectrum 2718 is an example spectrum for signal 2633 given the 200 MHZ clock with the aperture T_A = 500 psec (where 500 psec is π radians at the 5th harmonic of 1GHz). Similarly, the frequency spectrum 2720 is an example spectrum for signal 2633 given a 200 MHZ clock that is a square wave (so T_A = 5000 psec). The spectrum 2718 includes multiple harmonics 2718a-i, and the frequency spectrum 2720 includes multiple harmonics 2720a-e. [It is noted that spectrum 2720 includes only the odd harmonics as predicted by Fourier analysis for a square wave.] At 1 Ghz (which is the 5th harmonic), the signal amplitude of the two frequency spectrums 2718e and 2720c are approximately equal. However, at 200 MHZ, the frequency spectrum 2718a has a much lower amplitude than the frequency spectrum 2720a, and therefore the frequency spectrum 2718 is more efficient than the frequency spectrum 2720, assuming the desired harmonic is the 5th harmonic. In other words, assuming 1 Ghz is the desired harmonic, the frequency spectrum 2718 wastes less energy at the 200 MHZ fundamental than does the frequency spectrum 2718.

7.1.3 Balanced Modulator Having a Shunt Configuration

FIG. 56A illustrates a universal transmitter 5600 that is a second embodiment of a universal transmitter having two balanced UFT modules in a shunt configuration. (In contrast, the balanced modulator 2604 can be described as having a series configuration based on the orientation of the UFT modules.) Transmitter 5600 includes a balanced modulator 5601, the control signal generator 2642, the optional bandpass filter 2606, and the optional amplifier 2608. The transmitter 5600 up-converts a baseband signal 5602 to produce an output signal 5636 that is conditioned

1744 0450003

for wireless or wire line transmission. In doing so, the balanced modulator 5601 receives the baseband signal 5602 and shunts the baseband signal to ground in a differential and balanced fashion to generate a harmonically rich signal 5634. The harmonically rich signal 5634 includes multiple harmonic images, where each image contains the baseband information in the baseband signal 5602. In other words, each harmonic image includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 5602. The optional bandpass filter 2606 may be included to select a harmonic of interest (or a subset of harmonics) in the signal 5634 for transmission. The optional amplifier 2608 may be included to amplify the selected harmonic prior to transmission, resulting in the output signal 5636.

The balanced modulator 5601 includes the following components: a buffer/inverter 5604; optional impedances 5610, 5612; UFT modules 5616 and 5622 having controlled switches 5618 and 5624, respectively; blocking capacitors 5628 and 5630; and a terminal 5620 that is tied to ground. As stated above, the balanced modulator 5601 differentially shunts the baseband signal 5602 to ground, resulting in a harmonically rich signal 5634. More specifically, the UFT modules 5616 and 5622 alternately shunts the baseband signal to terminal 5620 according to control signals 2623 and 2627, respectively. Terminal 5620 is tied to ground and prevents any DC offset voltages from developing between the UFT modules 5616 and 5622. As described above, a DC offset voltage can lead to undesired carrier insertion. The operation of the balanced modulator 5601 is described in greater detail according to the flowchart 6400 (FIG. 64) as follows.

In step 6402, the buffer/inverter 5604 receives the input baseband signal 5602 and generates I signal 5606 and inverted I signal 5608. I signal 5606 is substantially similar to the baseband signal 5602, and the inverted I signal 5608 is an inverted version of signal 5602. As such, the buffer/inverter 5604 converts the (single-ended) baseband signal 5602 into differential signals 5606 and 5608 that are sampled by the UFT modules. Buffer/inverter 5604 can be implemented using known operational

amplifier (op amp) circuits, as will be understood by those skilled in the arts, although the invention is not limited to this example.

In step 6404, the control signal generator 2642 generates control signals 2623 and 2627 from the master clock signal 2645. Examples of the master clock signal 2645, control signal 2623, and control signal 2627 are shown in FIGs. 27A-C, respectively. As illustrated, both control signals 2623 and 2627 have the same period T_S as a master clock signal 2645, but have a pulse width (or aperture) of T_A. Control signal 2623 triggers on the rising pulse edge of the master clock signal 2645, and control signal 2627 triggers on the falling pulse edge of the master clock signal 2645. Therefore, control signals 2623 and 2627 are shifted in time by 180 degrees relative to each other. A specific embodiment of the control signal generator 2642 is illustrated in FIG. 26A, and was discussed in detail above.

In step 6406, the UFT module 5616 shunts the signal 5606 to ground according to the control signal 2623, to generate a harmonically rich signal 5614. More specifically, the switch 5618 closes and shorts the signal 5606 to ground (at terminal 5620) during the aperture width T_A of the control signal 2623, to generate the harmonically rich signal 5614. FIG. 56B illustrates an exemplary frequency spectrum for the harmonically rich signal 5618 having harmonic images 5650a-n. The images 5650 repeat at harmonics of the sampling frequency $1/T_S$, at infinitum, where each image 5650 contains the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 5602. The generation of harmonically rich signals by sampling an input signal according to a controlled aperture have been described earlier in this application in the section titled, "Frequency Up-conversion Using Universal Frequency Translation", and is illustrated by FIGs. 3-6. A more detailed discussion of frequency up-conversion using a switch with a controlled sampling aperture is discussed in the co-pending patent application titled, "Method and System for Frequency Up-Conversion," Ser. No./09/176,154, field on October 21, 1998, and incorporated herein by reference.

1744.0450003

The relative amplitude of the frequency images 5650 is generally a function of the harmonic number and the pulse width T_A. As such, the relative amplitude of a particular harmonic 5650 can be increased (or decreased) by adjusting the pulse width T_A of the control signal 2623. In general, shorter pulse widths of T_A shift more energy into the higher frequency harmonics, and longer pulse widths of T_A shift energy into the lower frequency harmonics. Additionally, the relative amplitude of a particular harmonic 5650 can also be adjusted by adding/tuning an optional impedance 5610. Impedance 5610 operates as a filter that emphasizes a particular harmonic in the harmonically rich signal 5614.

In step 6408, the UFT module 5622 shunts the inverted signal 5608 to ground according to the control signal 2627, to generate a harmonically rich signal 5626. More specifically, the switch 5624 closes during the pulse widths T_A and shorts the inverted I signal 5608 to ground (at terminal 5620), to generate the harmonically rich signal 5626. At any given time, only one of input signals 5606 or 5608 is shorted to ground because the pulses in the control signals 2623 and 2627 are phase shifted with respect to each other, as shown in FIGs. 27B and 27C.

The harmonically rich signal 5626 includes multiple frequency images of baseband signal 5602 that repeat at harmonics of the sampling frequency $(1/T_S)$, similar to that for the harmonically rich signal 5614. However, the images in the signal 5626 are phase-shifted compared to those in signal 5614 because of the inversion of the signal 5608 compared to the signal 5606, and because of the relative phase shift between the control signals 2623 and 2627. The optional impedance 5612 can be included to emphasis a particular harmonic of interest, and is similar to the impedance 5610 above.

In step 6410, the node 5632 sums the harmonically rich signals 5614 and 5626 to generate the harmonically rich signal 5634. The capacitors 5628 and 5630 operate as blocking capacitors that substantially pass the respective harmonically rich signals 5614 and 5626 to the node 5632 (The capacitor values may be chosen to

substantially block baseband frequency components as well.) FIG. 56C illustrates an exemplary frequency spectrum for the harmonically rich signal 5634 that has multiple images 5652a-n that repeat at harmonics of the sampling frequency $1/T_S$. Each image 5652 includes the necessary amplitude, frequency, and phase information to reconstruct the baseband signal 5602. The optional filter 2606 can be used to select the harmonic image of interest for transmission. This is represented by a passband 5656 that selects the harmonic image 5632c for transmission.

An advantage of the modulator 5601 is that it is fully balanced, which substantially minimizes (or eliminates) any DC voltage offset between the two UFT modules 5612 and 5614. DC offset is minimized because the UFT modules 5616 and 5622 are both connected to ground at terminal 5620. The result of controlling the DC offset between the UFT modules is that carrier insertion is minimized in the harmonic images of the harmonically rich signal 5634. As discussed above, carrier insertion is substantially wasted energy because the information for a modulated signal is carried in the sidebands of the modulated signal and not in the carrier. Therefore, it is often desirable to minimize the energy at the carrier frequency by controlling the relative DC offset.

7.1.4   Balanced Modulator FET Configuration

As described above, the balanced modulators 2604 and 5601 utilize two balanced UFT modules to sample the input baseband signals to generate harmonically rich signals that contain the up-converted baseband information. More specifically, the UFT modules include controlled switches that sample the baseband signal in a balanced and differential fashion. FIGs. 26D and 56D illustrate embodiments of the controlled switch in the UFT module.

FIG. 26D illustrates an example embodiment of the modulator 2604 (FIG. 26B) where the controlled switches in the UFT modules are field effect transistors

(FET). More specifically, the controlled switches 2648 and 2628 are embodied as FET 2658 and FET 2660, respectively. The FET 2658 and 2660 are oriented so that their gates are controlled by the control signals 2623 and 2627, so that the control signals control the FET conductance. For the FET 2658, the combined baseband signal 2620 is received at the source of the FET 2658 and is sampled according to the control signal 2623 to produce the harmonically rich signal 2630 at the drain of the FET 2658. Likewise, the combined baseband signal 2622 is received at the source of the FET 2660 and is sampled according to the control signal 2627 to produce the harmonically rich signal 2634 at the drain of FET 2660. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs. In other words, the combined baseband signal can be received at the drain of the FETs, and the harmonically rich signals can be taken from the source of the FETs, as will be understood by those skilled in the relevant arts.

FIG. 56D illustrates an embodiment of the modulator 5600 (FIG. 56) where the controlled switches in the UFT modules are field effect transistors (FET). More specifically, the controlled switches 5618 and 5624 are embodied as FET 5636 and FET 5638, respectively. The FETs 5636 and 5638 are oriented so that their gates are controlled by the control signals 2623 and 2627, respectively, so that the control signals determine FET conductance. For the FET 5636, the baseband signal 5606 is received at the source of the FET 5636 and shunted to ground according to the control signal 2623, to produce the harmonically rich signal 5614. Likewise, the baseband signal 5608 is received at the source of the FET 5638 and is shunted to grounding according to the control signal 2627, to produce the harmonically rich signal 5626. The source and drain orientation that is illustrated is not limiting, as the source and drains can be switched for most FETs, as will be understood by those skilled in the relevant arts.

7.1.5 Universal Transmitter Configured for Carrier Insertion

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As discussed above, the transmitters 2602 and 5600 have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the output signal 2640. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, the present invention can be configured to provide the necessary carrier insertion by implementing a DC offset between the two sampling UFT modules.

FIG. 28A illustrates a transmitter 2802 that up-converts a baseband signal 2806 to an output signal 2822 having carrier insertion. As is shown, the transmitter 2802 is similar to the transmitter 2602 (FIG. 26A) with the exception that the up-converter/modulator 2804 is configured to accept two DC references voltages. In contrast, modulator 2604 was configured to accept only one DC reference voltage. More specifically, the modulator 2804 includes a terminal 2809 to accept a DC reference voltage 2808, and a terminal 2813 to accept a DC reference voltage 2814. Vr 2808 appears at the UFT module 2624 though summer amplifier 2618 and the inductor 2810. Vr 2814 appears at UFT module 2628 through the summer amplifier 2619 and the inductor 2816. Capacitors 2812 and 2818 operate as blocking capacitors. If Vr 2808 is different from Vr 2814 then a DC offset voltage will be exist between UFT module 2624 and UFT module 2628, which will be up-converted at the carrier frequency in the harmonically rich signal 2820. More specifically, each harmonic image in the harmonically rich signal 2820 will include a carrier signal as depicted in FIG. 28B.

FIG. 28B illustrates an exemplary frequency spectrum for the harmonically rich signal 2820 that has multiple harmonic images 2824a-n. In addition to carrying the baseband information in the sidebands, each harmonic image 2824 also includes a carrier signal 2826 that exists at respective harmonic of the sampling frequency

$1/T_s$. The amplitude of the carrier signal increases with increasing DC offset voltage. Therefore, as the difference between Vr 2808 and Vr 2814 widens, the amplitude of each carrier signal 2826 increases. Likewise, as the difference between Vr 2808 and Vr 2814 shrinks, the amplitude of each carrier signal 2826 shrinks. As with transmitter 2802, the optional bandpass filter 2606 can be included to select a desired harmonic image for transmission. This is represented by passband 2828 in FIG. 28B.

7.2   Universal Transmitter In I Q Configuration:

As described above, the balanced modulators 2604 and 5601 up-convert a baseband signal to a harmonically rich signal having multiple harmonic images of the baseband information. By combining two balanced modulators, IQ configurations can be formed for up-converting I and Q baseband signals. In doing so, either the (series type) balanced modulator 2604 or the (shunt type) balanced modulator can be utilized. IQ modulators having both series and shunt configurations are described below.

7.2.1   IQ Transmitter Using Series-Type Balanced Modulator

FIG. 29 illustrates an IQ transmitter 2920 with an in-phase (I) and quadrature (Q) configuration according to embodiments of the invention. The transmitter 2920 includes an IQ balanced modulator 2910, an optional filter 2914, and an optional amplifier 2916. The transmitter 2920 is useful for transmitting complex I Q waveforms and does so in a balanced manner to control DC offset and carrier insertion. In doing so, the modulator 2910 receives an I baseband signal 2902 and a Q baseband signal 2904 and up-converts these signals to generate a combined harmonically rich signal 2912. The harmonically rich signal 2912 includes multiple harmonics images, where each image contains the baseband information in the I signal

1744.0450003

2902 and the Q signal 2904. The optional bandpass filter 2914 may be included to select a harmonic of interest (or subset of harmonics) from the signal 2912 for transmission. The optional amplifier 2916 may be included to amplify the selected harmonic prior to transmission, to generate the IQ output signal 2918.

5   As stated above, the balanced IQ modulator 2910 up-converts the I baseband signal 2902 and the Q baseband signal 2904 in a balanced manner to generate the combined harmonically rich signal 2912 that carriers the I and Q baseband information. To do so, the modulator 2910 utilizes two balanced modulators 2604 from FIG. 26A, a signal combiner 2908, and a DC terminal 2907. The operation of

10   the balanced modulator 2910 and other circuits in the transmitter is described according to the flowchart 6500 in FIG. 65, as follows.

In step 6502, the IQ modulator 2910 receives the I baseband signal 2902 and the Q baseband signal 2904.

In step 6504, the I balanced modulator 2604a samples the I baseband signal 2902 in a differential fashion using the control signals 2623 and 2627 to generate a

15   harmonically rich signal 2911a. The harmonically rich signal 2911a contains multiple harmonic images of the I baseband information, similar to the harmonically rich signal 2630 in FIG. 26B.

In step 6506, the balanced modulator 2604b samples the Q baseband signal

20   2904 in a differential fashion using control signals 2623 and 2627 to generate harmonically rich signal 2911b, where the harmonically rich signal 2911b contains multiple harmonic images of the Q baseband signal 2904. The operation of the balanced modulator 2604 and the generation of harmonically rich signals was fully described above and illustrated in FIGs. 26A-C, to which the reader is referred for

25   further details.

In step 6508, the DC terminal 2907 receives a DC voltage 2906 that is distributed to both modulators 2604a and 2604b. The DC voltage 2906 is distributed to both the input and output of both UFT modules 2624 and 2628 in each modulator

2604. This minimizes (or prevents) DC offset voltages from developing between the four UFT modules, and thereby minimizes or prevents any carrier insertion during the sampling steps 6504 and 6506.

In step 6510, the 90 degree signal combiner 2908 combines the harmonically rich signals 2911a and 2911b to generate IQ harmonically rich signal 2912. This is further illustrated in FIGs. 30A-C. FIG. 30A depicts an exemplary frequency spectrum for the harmonically rich signal 2911a having harmonic images 3002a-n. The images 3002 repeat at harmonics of the sampling frequency $1/T_S$, where each image 3002 contains the necessary amplitude and frequency information to reconstruct the I baseband signal 2902. Likewise, FIG. 30B depicts an exemplary frequency spectrum for the harmonically rich signal 2911b having harmonic images 3004a-n. The harmonic images 3004a-n also repeat at harmonics of the sampling frequency $1/T_S$, where each image 3004 contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal 2904. FIG.30C illustrates an exemplary frequency spectrum for the combined harmonically rich signal 2912 having images 3006. Each image 3006 carries the I baseband information and the Q baseband information from the corresponding images 3002 and 3004, respectively, without substantially increasing the frequency bandwidth occupied by each harmonic 3006. This can occur because the signal combiner 2908 phase shifts the Q signal 2911b by 90 degrees relative to the I signal 2911a. The result is that the images 3002a-n and 3004a-n effectively share the signal bandwidth do to their orthogonal relationship. For example, the images 3002a and 3004a effectively share the frequency spectrum that is represented by the image 3006a.

In step 6512, the optional filter 2914 can be included to select a harmonic of interest, as represented by the passband 3008 selecting the image 3006c in FIG. 30c.

In step 6514, the optional amplifier 2916 can be included to amplify the harmonic (or harmonics) of interest prior to transmission.

1744.0450003

In step 6516, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. 31A illustrates a transmitter 3108 that is a second embodiment for an I Q transmitter having a balanced configuration. Transmitter 3108 is similar to the transmitter 2920 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays 3104a and 3104b delay the control signals 2623 and 2627 for the Q channel modulator 2604b by 90 degrees relative the control signals for the I channel modulator 2604a. As a result, the Q modulator 2604b samples the Q baseband signal 2904 with 90 degree delay relative to the sampling of the I baseband signal 2902 by the I channel modulator 2604a. Therefore, the Q harmonically rich signal 2911b is phase shifted by 90 degrees relative to the I harmonically rich signal. Since the phase shift is achieved using the control signals, an in-phase signal combiner 3106 combines the harmonically rich signals 2911a and 2911b, to generate the harmonically rich signal 2912.

FIG. 31B illustrates a transmitter 3118 that is similar to transmitter 3108 in FIG. 31A. The difference being that the transmitter 3118 has a modulator 3120 that utilizes a summing node 3122 to sum the signals 2911a and 2911b instead of the in-phase signal combiner 3106 that is used in modulator 3102 of transmitter 3108.

FIG. 55A-55D illustrate various detailed circuit implementations of the transmitter 2920 in FIG. 29. These circuit implementations are meant for example purposes only, and are not meant to be limiting.

FIG. 55A illustrates I input circuitry 5502a and Q input circuitry 5502b that receive the I and Q input signals 2902 and 2904, respectively.

FIG. 55B illustrates the I channel circuitry 5506 that processes an I data 5504a from the I input circuit 5502a.

FIG. 55C illustrates the Q channel circuitry 5508 that processes the Q data 5504b from the Q input circuit 5502b.

FIG. 55D illustrates the output combiner circuit 5512 that combines the I channel data 5507 and the Q channel data 5510 to generate the output signal 2918.

7.2.2. IQ Transmitter Using Shunt-Type Balanced Modulator

FIG. 57 illustrates an IQ transmitter 5700 that is another IQ transmitter embodiment according to the present invention. The transmitter 5700 includes an IQ balanced modulator 5701, an optional filter 5712, and an optional amplifier 5714. During operation, the modulator 5701 up-converts an I baseband signal 5702 and a Q baseband signal 5704 to generate a combined harmonically rich signal 5711. The harmonically rich signal 5711 includes multiple harmonics images, where each image contains the baseband information in the I signal 5702 and the Q signal 5704. The optional bandpass filter 5712 may be included to select a harmonic of interest (or subset of harmonics) from the harmonically rich signal 5711 for transmission. The optional amplifier 5714 may be included to amplify the selected harmonic prior to transmission, to generate the IQ output signal 5716.

The IQ modulator 5701 includes two balanced modulators 5601 from FIG. 56, and a 90 degree signal combiner 5710 as shown. The operation of the IQ modulator 5701 is described in reference to the flowchart 6600 (FIG. 66), as follows. The order of the steps in flowchart 6600 is not limiting.

In step 6602, the balanced modulator 5701 receives the I baseband signal 5702 and the Q baseband signal 5704.

In step 6604, the balanced modulator 5601a differentially shunts the I baseband signal 5702 to ground according the control signals 2623 and 2627, to generate a harmonically rich signal 5706. More specifically, the UFT modules 5616a and 5622a alternately shunt the I baseband signal and an inverted version of the I baseband signal to ground according to the control signals 2623 and 2627, respectively. The operation of the balanced modulator 5601 and the generation of

harmonically rich signals was fully described above and is illustrated in FIGs. 56A-C, to which the reader is referred for further details. As such, the harmonically rich signal 5706 contains multiple harmonic images of the I baseband information as described above.

In step 6606, the balanced modulator 5601b differentially shunts the Q baseband signal 5704 to ground according to control signals 2623 and 2627, to generate harmonically rich signal 5708. More specifically, the UFT modules 5616b and 5622b alternately shunt the Q baseband signal and an inverted version of the Q baseband signal to ground, according to the control signals 2623 and 2627, respectively. As such, the harmonically rich signal 5708 contains multiple harmonic images that contain the Q baseband information.

In step 6608, the 90 degree signal combiner 5710 combines the harmonically rich signals 5706 and 5708 to generate IQ harmonically rich signal 5711. This is further illustrated in FIGs. 58A-C. FIG. 58A depicts an exemplary frequency spectrum for the harmonically rich signal 5706 having harmonic images 5802a-n. The harmonic images 5802 repeat at harmonics of the sampling frequency $1/T_S$, where each image 5802 contains the necessary amplitude, frequency, and phase information to reconstruct the I baseband signal 5702. Likewise, FIG. 58B depicts an exemplary frequency spectrum for the harmonically rich signal 5708 having harmonic images 5804a-n. The harmonic images 5804a-n also repeat at harmonics of the sampling frequency $1/T_S$, where each image 5804 contains the necessary amplitude, frequency, and phase information to reconstruct the Q baseband signal 5704. FIG. 58C illustrates an exemplary frequency spectrum for the IQ harmonically rich signal 5711 having images 5806a-n. Each image 5806 carries the I baseband information and the Q baseband information from the corresponding images 5802 and 5804, respectively, without substantially increasing the frequency bandwidth occupied by each image 5806. This can occur because the signal combiner 5710 phase shifts the Q signal 5708 by 90 degrees relative to the I signal 5706.

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Inn step 6610, the optional filter 5712 may be included to select a harmonic of interest, as represented by the passband 5808 selecting the image 5806c in FIG. 58C.

In step 6612, the optional amplifier 5714 can be included to amplify the selected harmonic image 5806 prior to transmission.

In step 6614, the selected harmonic (or harmonics) is transmitted over a communications medium.

FIG. 59 illustrates a transmitter 5900 that is another embodiment for an I Q transmitter having a balanced configuration. Transmitter 5900 is similar to the transmitter 5700 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals instead of using a 90 degree signal combiner to combine the harmonically rich signals. More specifically, delays 5904a and 5904b delay the control signals 2623 and 2627 for the Q channel modulator 5601b by 90 degrees relative the control signals for the I channel modulator 5601a. As a result, the Q modulator 5601b samples the Q baseband signal 5704 with a 90 degree delay relative to the sampling of the I baseband signal 5702 by the I channel modulator 5601a. Therefore, the Q harmonically rich signal 5708 is phase shifted by 90 degrees relative to the I harmonically rich signal 5706. Since the phase shift is achieved using the control signals, an in-phase signal combiner 5906 combines the harmonically rich signals 5706 and 5708, to generate the harmonically rich signal 5711.

FIG. 60 illustrates a transmitter 6000 that is similar to transmitter 5900 in FIG. 59. The difference being that the transmitter 6000 has a balanced modulator 6002 that utilizes a summing node 6004 to sum the I harmonically rich signal 5706 and the Q harmonically rich signal 5708 instead of the in-phase signal combiner 5906 that is used in the modulator 5902 of transmitter 5900. The 90 degree phase shift between the I and Q channels is implemented by delaying the Q clock signals using 90 degree delays 5904, as shown.

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7.2.3 IQ Transmitters Configured for Carrier Insertion

The transmitters 2920 (FIG. 29) and 3108 (FIG. 31A) have a balanced configuration that substantially eliminates any DC offset and results in minimal carrier insertion in the IQ output signal 2918. Minimal carrier insertion is generally desired for most applications because the carrier signal carries no information and reduces the overall transmitter efficiency. However, some applications require the received signal to have sufficient carrier energy for the receiver to extract the carrier for coherent demodulation. In support thereof, FIG. 32 illustrates a transmitter 3202 to provide any necessary carrier insertion by implementing a DC offset between the two sets of sampling UFT modules.

Transmitter 3202 is similar to the transmitter 2920 with the exception that a modulator 3204 in transmitter 3202 is configured to accept two DC reference voltages so that the I channel modulator 2604a can be biased separately from the Q channel modulator 2604b. More specifically, modulator 3204 includes a terminal 3206 to accept a DC voltage reference 3207, and a terminal 3208 to accept a DC voltage reference 3209. Voltage 3207 biases the UFT modules 2624a and 2628a in the I channel modulator 2604a. Likewise, voltage 3209 biases the UFT modules 2624b and 2628b in the Q channel modulator 2604b. When voltage 3207 is different from voltage 3209, then a DC offset will appear between the I channel modulator 2604a and the Q channel modulator 2604b, which results in carrier insertion in the IQ harmonically rich signal 2912. The relative amplitude of the carrier frequency energy increases in proportion to the amount of DC offset.

FIG. 33 illustrates a transmitter 3302 that is a second embodiment of an IQ transmitter having two DC terminals to cause DC offset, and therefore carrier insertion. Transmitter 3302 is similar to transmitter 3202 except that the 90 degree phase shift between the I and Q channels is achieved by phase shifting the control signals, similar to that done in transmitter 3108. More specifically, delays 3304a and

3304b phase shift the control signals 2623 and 2627 for the Q channel modulator 2604b relative to those of the I channel modulator 2604a. As a result, the Q modulator 2604b samples the Q baseband signal 2904 with 90 degree delay relative to the sampling of the I baseband signal 2902 by the I channel modulator 2604a. Therefore, the Q harmonically rich signal 2911b is phase shifted by 90 degrees relative to the I harmonically rich signal, which is then combined by the in-phase combiner 3306.

7.3 Universal Transmitter and CDMA

The universal transmitter 2920 (FIG. 29) and the universal transmitter 5700 (FIG. 57) can be used to up-convert every known useful analog and digital baseband waveform including but not limited to: AM, FM, PM, BPSK, QPSK, MSK, QAM, ODFM, multi-tone, and spread spectrum signals. For further illustration, FIG. 34A and FIG. 34B depict transmitter 2920 configured to up-convert the mentioned modulation waveforms. FIG. 34A illustrates transmitter 2920 configured to up-convert non-complex waveform including AM and shaped BPSK. In FIG. 34A, these non-complex (and non-IQ) waveforms are received on the I terminal 3402, and the Q input 3404 is grounded since only a single channel is needed. FIG. 34B illustrates a transmitter 2920 that is configured to receive both I and Q inputs for the up-conversion of complex waveforms including QPSK, QAM, OFDM, GSM, and spread spectrum waveforms (including CDMA and frequency hopping). The transmitters in FIGs. 34A and 34B are presented for illustrative purposes, and are not limiting. Other embodiments are possible, as will be appreciated in view of the teachings herein.

CDMA is an input waveform that is of particular interest for communications applications. CDMA is the fastest growing digital cellular communications standard in many regions, and now is widely accepted as the foundation for the competing third generation (3G) wireless standard. CDMA is considered to be the among the most

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demanding of the current digital cellular standards in terms of RF performance requirements.

7.3.1   IS-95 CDMA Specifications

FIG. 35A and FIG. 35B illustrate the CDMA specifications for base station and mobile transmitters as required by the IS-95 standard. FIG. 35A illustrates a base station CDMA signal 3502 having a main lobe 3504 and sidelobes 3506a and 3506b. For base station transmissions, IS-95 requires that the sidelobes 3506a,b are at least 45 dB below the mainlobe 3504 (or 45dbc) at an offset frequency of 750 kHz, and 60dBc at an offset frequency of 1.98 MHZ. FIG. 35B illustrates similar requirements for a mobile CDMA signal 3508 having a main lobe 3510 and sidelobes 3512a and 3512b. For mobile transmissions, CDMA requires that the sidelobes 3512a,b are at least 42 dBc at a frequency offset of 885 kHz, and 54 dBc at a frequency offset 1.98 MHZ.

Rho is another well known performance parameter for CDMA . Rho is a figure-of-merit that measures the amplitude and phase distortion of a CDMA signal that has been processed in some manner (e.g. amplified, up-converted, filtered, etc.) The maximum theoretical value for Rho is 1.0, which indicates no distortion during the processing of the CDMA signal. The IS-95 requirement for the baseband-to-RF interface is Rho= .9912. As will be shown by the test results below, the transmitter 2920 (in FIG. 29) can up-convert a CDMA baseband signal and achieve Rho values of approximately Rho= 0.9967. Furthermore, the modulator 2910 in the transmitter 2920 achieves these results in standard CMOS (although the invention is not limited to this example implementation), without doing multiple up-conversions and IF filtering that is associated with conventional super-heterodyne configurations.

7.3.2   Conventional CDMA Transmitter

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Before describing the CDMA implementation of transmitter 2920, it is useful to describe a conventional super-heterodyne approach that is used to meet the IS-95 specifications. FIG. 36 illustrates a conventional CDMA transmitter 3600 that up-converts an input signal 3602 to an output CDMA signal 3634. The conventional CDMA transmitter 3600 includes: a baseband processor 3604, a baseband filter 3608, a first mixer 3612, an amplifier 3616, a SAW filter 3620, a second mixer 3624, a power amplifier 3628, and a band-select filter 3632. The conventional CDMA transmitter operates as follows.

The baseband processor 3604 spreads the input signal 3602 with I and Q spreading codes to generate I signal 3606a and Q signal 3606b, which are consistent with CDMA IS-95 standards. The baseband filter 3608 filters the signals 3606 with the aim of reducing the sidelobes so as to meet the sidelobe specifications that were discussed in FIGs. 35A and 35B. Mixer 3612 up-converts the signal 3610 using a first LO signal 3613 to generate an IF signal 3614. IF amplifier 3616 amplifies the IF signal 3614 to generate IF signal 3618. SAW filter 3620 has a bandpass response that filters the IF signal 3618 to suppress any sidelobes caused by the non-linear operations of the mixer 3614. As is understood by those skilled in the arts, SAW filters provide significant signal suppression outside the passband, but are relatively expensive and large compared to other transmitter components. Furthermore, SAW filters are typically built on specialized materials that cannot be integrated onto a standard CMOS chip with other components. Mixer 3624 up-converts the signal 3622 using a second LO signal 3625 to generate RF signal 3626. Power amplifier 3628 amplifies RF signal 3626 to generate signal 3630. Band-select filter 3632 bandpass filters RF signal 3630 to suppress any unwanted harmonics in output signal 3634.

It is noted that transmitter 3602 up-converts the input signal 3602 using an IF chain 3636 that includes the first mixer 3612, the amplifier 3616, the SAW filter 3620, and the second mixer 3624. The IF chain 3636 up-converts the input signal to an IF frequency and does IF amplification and SAW filtering in order to meet the IS-95

sidelobe and figure-of-merit specifications. This is done because conventional wisdom teaches that a CDMA baseband signal cannot be up-converted directly from baseband to RF, and still meet the IS-95 linearity requirements.

7.3.3   CDMA Transmitter Using the Present Invention

For comparison, FIG. 37A illustrates an example CDMA transmitter 3700 according to embodiments of the present invention. The CDMA transmitter 3700 includes (it is noted that the invention is not limited to this example): the baseband processor 3604; the baseband filter 3608; the IQ modulator 2910 (from FIG. 29), the control signal generator 2642, the sub-harmonic oscillator 2646, the power amplifier 3628, and the filter 3632. In the example of FIG. 37A, the baseband processor 3604, baseband filter 3608, amplifier 3628, and the band-select filter 3632 are the same as that used in the conventional transmitter 3602 in FIG.36. The difference is that the IQ modulator 2910 in transmitter 3700 completely replaces the IF chain 3636 in the conventional transmitter 3602. This is possible because the modulator 2910 up-converts a CDMA signal directly from baseband-to-RF without any IF processing. The detailed operation of the CDMA transmitter 3700 is described with reference to the flowchart 7300 (FIG. 73) as follows.

In step 7302, the input baseband signal 3702 is received.

In step 7304, the CDMA baseband processor 3604 receives the input signal 3702 and spreads the input signal 3702 using I and Q spreading codes, to generate an I signal 3704a and a Q signal 3704b. As will be understood, the I spreading code and Q spreading codes can be different to improve isolation between the I and Q channels.

In step 7306, the baseband filter 3608 bandpass filters the I signal 3704a and the Q signal 3704b to generate filtered I signal 3706a and filtered Q signal 3706b. As mentioned above, baseband filtering is done to improve sidelobe suppression in the CDMA output signal.

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FIGs. 37B- 37D illustrate the effect of the baseband filter 3608 on the I an Q inputs signals. FIG. 37B depicts multiple signal traces (over time) for the filtered I signal 3706a, and FIG. 37C depicts multiple signal traces for the filtered Q signal 3706b. As shown, the signals 3706a,b can be described as having an "eyelid" shape having a thickness 3715. The thickness 3715 reflects the steepness of passband roll off of the baseband filter 3608. In other words, a relatively thick eyelid in the time domain reflects a steep passband roll off in the frequency domain, and results in lower sidelobes for the output CDMA signal. However, there is a tradeoff, because as the eyelids become thicker, then there is a higher probability that channel noise will cause a logic error during decoding at the receiver. The voltage rails 3714 represent the +1/-1 logic states for the I and Q signals 3706, and correspond to the logic states in complex signal space that are shown in FIG. 37D.

In step 7308, the IQ modulator 2910 samples I and Q input signals 3706A, 3706B in a differential and balanced fashion according to sub-harmonic clock signals 2623 and 2627, to generate a harmonically rich signal 3708. FIG 37E illustrates the harmonically rich signal 3708 that includes multiple harmonic images 3716a-n that repeat at harmonics of the sampling frequency $1/T_s$. Each image 3716a-n is a spread spectrum signal that contains the necessary amplitude, frequency, and phase information to reconstruct the input baseband signal 3702.

In step 7310, the amplifier 3628 amplifies the harmonically rich signal 3708 to generate an amplified harmonically rich signal 3710.

Finally, the band-select filter 3632 selects the harmonic of interest from signal 3710, to generate an CDMA output signal 3712 that meets IS-95 CDMA specifications. This is represented by passband 3718 selecting harmonic image 3716b in FIG. 37E.

An advantage of the CDMA transmitter 3700 is in that the modulator 2910 up-converts a CDMA input signal directly from baseband to RF without any IF processing, and still meets the IS-95 sidelobe and figure-of-merit specifications. In

other words, the modulator 2910 is sufficiently linear and efficient during the up-conversion process that no IF filtering or amplification is required to meet the IS-95 requirements. Therefore, the entire IF chain 3636 can be replaced by the modulator 2910, including the expensive SAW filter 3620. Since the SAW filter is eliminated, substantial portions of the transmitter 3702 can be integrated onto a single CMOS chip, for example, that uses standard CMOS process More specifically, and for illustrative purposes only, the baseband processor 3604, the baseband filter 3608, the modulator 2910, the oscillator 2646,and the control signal generator 2642 can be integrated on a single CMOS chip, as illustrated by CMOS chip 3802 in FIG. 38, although the invention is not limited to this implementation example.

FIG. 37F illustrates a transmitter 3720 that is similar to transmitter 3700 (FIG. 37A) except that modulator 5701 replaces the modulator 2910. Transmitter 3700 operates similar to the transmitter 3700 and has all the same advantages of the transmitter 3700.

Other embodiments discussed or suggested herein can be used to implement other CDMA transmitters according to the invention.

7.3.4   CDMA Transmitter Measured Test Results

As discussed above, the UFT-based modulator 2910 directly up-converts baseband CDMA signals to RF without any IF filtering, while maintaining the required figures-of-merit for IS-95. The modulator 2910 has been extensively tested in order to specifically determine the performance parameters when up-converting CDMA signals. The test system and measurement results are discussed as follows.

FIG. 39 illustrates a test system 3900 that measures the performance of the modulator 2910 when up-converting CDMA baseband signals. The test system 3900 includes: a Hewlett Packerd (HP) generator E4433B, attenuators 3902a and 3902b, control signal generator 2642, UFT-based modulator 2910, amplifier/filter module

3904, cable/attenuator 3906, and HP 4406A test set. The HP generator E4433B generates I and Q CDMA baseband waveforms that meet the IS-95 test specifications. The waveforms are routed to the UFT-based modulator 2910 through the 8-dB attenuators 3902a and 3902b. The HP generator E4433B also generates the sub-harmonic clock signal 2645 that triggers the control signal generator 2642, where the sub-harmonic clock 2645 has a frequency of 279 MHZ. The modulator 2910 up-converts the I and Q baseband signals to generate a harmonic rich signal 3903 having multiple harmonic images that represent the input baseband signal and repeat at the sampling frequency. The amplifier/filter module 3904 selects and amplifies the 3rd harmonic (of the 279 MHZ clock signal) in the signal 3903 to generate the signal 3905 at 837 MHZ. The HP 4406A test set accepts the signal 3905 for analysis through the cable/attenuator 3906. The HP 4406A measures CDMA modulation attributes including: Rho, EVM, phase error, amplitude error, output power, carrier insertion, and ACPR. In addition, the signal is demodulated and Walsh code correlation parameters are analyzed. Both forward and reverse links have been characterized using pilot, access, and traffic channels. For further illustration, FIGs. 40-60Z display the measurement results for the RF spectrum 3905 based on various base station and mobile waveforms that are generated by the HP E443B generator.

FIGs. 40 and 41 summarize the performance parameters of the modulator 2910 as measured by the test set 3900 for base station and mobile station input waveforms, respectively. For the base station, table 4002 includes lists performance parameters that were measured at a base station middle frequency and includes: Rho, EVM, phase error, magnitude error, carrier insertion, and output power. It is noted that Rho= .997 for the base station middle frequency and exceeds the IS-95 requirement of Rho= 0.912. For the mobile station, FIG. 41 illustrates a table 4102 that lists performance parameters that were measured at low, middle, and high frequencies. It is noted that the Rho exceeds the IS-95 requirement (0.912) for each of the low, middle, high frequencies of the measured waveform.

FIG. 42 illustrates a base station constellation 4202 measured during a pilot channel test. A signal constellation plots the various logic combinations for the I and Q signals in complex signal space, and is the raw data for determining the performance parameters (including Rho) that are listed in Table 40. The performance parameters (in table 40) are also indicated beside the constellation measurement 4202 for convenience. Again, it is noted that Rho= 0.997 for this test. A value of 1 is perfect, and 0.912 is required by the IS-95 CDMA specification, although most manufactures strive for values greater than 0.94. This is a remarkable result since the modulator 2910 up-converts directly from baseband-to-RF without any IF filtering.

FIG. 43 illustrates a base station sampled constellation 4302, and depicts the tight constellation samples that are associated with FIG. 42. The symmetry and sample scatter compactness are illustrative of the superior performance of the modulator 2910.

FIG. 44 illustrates a mobile station constellation 4402 measured during an access channel test. As shown, Rho= 0.997 for the mobile station waveforms. Therefore, the modulator 2910 operates very well with conventional and offset shaped QPSK modulation schemes.

FIG. 45 illustrates a mobile station sampled constellation 4502. Constellation 4502 illustrates excellent symmetry for the constellation sample scatter diagram.

FIG. 46 illustrates a base station constellation 4602 using only the HP test equipment. The modulator 2910 has been removed so that the base station signal travels only through the cables that connect the HP signal generator E4433B to the HP 4406A test set. Therefore, constellation 4602 measures signal distortion caused by the test set components (including the cables and the attenuators). It is noted that Rho=0.9994 for this measurement using base station waveforms. Therefore, at least part of the minimal signal distortion that is indicated in FIGs. 42 and 43 is caused by the test set components, as would be expected by those skilled in the relevant arts.

FIG. 47 illustrates a mobile station constellation 4702 using only the HP test equipment. As in FIG. 46, the modulator 2910 has been removed so that the mobile station signal travels only through the cables that connect the HP signal generator E4433B to the HP 4406A test set. Therefore, constellation 4602 measures signal distortion caused by the test set components (including the cables and the attenuators). It is noted that Rho=0.9991 for this measurement using mobile station waveforms. Therefore, at least part of the signal distortion indicated in FIGs. 44 and 45 is caused by the test set components, as would be expected.

FIG. 48 illustrates a frequency spectrum 4802 of the signal 3905 with a base station input waveform. The frequency spectrum 4802 has a main lobe and two sidelobes, as expected for a CDMA spread spectrum signal. The adjacent channel power ratio (ACPR) measures the spectral energy at a particular frequency of the side lobes relative to the main lobe. As shown, the frequency spectrum 4802 has an ACPR= -48.34 dBc and -62.18 dBc at offset frequencies of 750 KHz and 1.98 MHZ, respectively. The IS-95 ACPR requirement for a base station waveform is -45dBc and -60 dBc maximum, at the offset frequencies of 750 kHz and 1.98 MHZ, respectively. Therefore, the modulator 2910 has more than 3dB and 2 dB of margin over the IS-95 requirements for the 750 kHz and 1.98 MHZ offsets, respectively.

FIG. 49 illustrates a histogram 4902 that corresponds to the spectrum plot in FIG. 48. The histogram 4902 illustrates the distribution of the spectral energy in the signal 3905 for a base station waveform.

FIG. 50 illustrates a frequency spectrum 5002 of the signal 3905 with a mobile station input waveform. As shown, the ACPR measurement is -52.62 dBc and -60.96 dBc for frequency offsets of 885 kHz and 1.98 MHZ, respectively. The IS-95 ACPR requirement for a mobile station waveform is approximately -42dBc and -54 dBc, respectively. Therefore, the modulator 2910 has over 10 dB and 6 dB of margin above the IS-95 requirements for the 885 kHz and 1.98 MHZ frequency offsets, respectively.

FIG. 51 illustrates a histogram 5102 that corresponds to the mobile station spectrum plot in FIG.50. The histogram 5102 illustrates the distribution of the spectral energy in the signal 3905 for a mobile station waveform.

FIG. 52A illustrates a histogram 5202 for crosstalk vs. CDMA channel with a base station input waveform. More specifically, the HP E4406A was utilized as a receiver to analyze the orthogonality of codes superimposed on the base station modulated spectrum. The HP E4406A demodulated the signal provided by the modulator/transmitter and determined the crosstalk to non-active CDMA channels. The pilot channel is in slot '0' and is the active code for this test. All non-active codes are suppressed in the demodulation process by greater than 40 dB. The IS-95 requirement is 27 dB of suppression so that there is over 13 dB of margin. This implies that the modulator 2910 has excellent phase and amplitude linearity.

In additions to the measurements described above, measurements were also conducted to obtain the timing and phase delays associated with a base station transmit signal composed of pilot and active channels. Delta measurements were extracted with the pilot signal as a reference. The delay and phase are -5.7 ns (absolute) and 7.5 milli radians, worst case. The standard requires less than 50 ns (absolute) and 50 milli radians, which the modulator 2910 exceeded with a large margin.

The performance sensitivity of modulator 2910 was also measured over multiple parameter variations. More specifically, the performance sensitivity was measured vs. IQ input signal level variation and LO signal level variation, for both base station and mobile station modulation schemes. (LO signal level is the signal level of the subharmonic clock 2645 in FIG. 39.) FIGs. 52B-O depict performance sensitivity of the modulator 2910 using the base station modulation scheme, and FIGs. 52P-Z depict performance sensitivity using the mobile station modulation scheme. These plots reveal that the modulator 2910 is expected to enable good production

yields since there is a large acceptable operating performance range for I/Q and LO peak to peak voltage inputs. The plots are described further as follows.

FIG. 52B illustrates Rho vs. shaped IQ input signal level using base station modulation.

FIG. 52C illustrates transmitted channel power vs. shaped IQ input signal level using base station modulation.

FIG. 52D illustrates ACPR vs shaped IQ Input signal level using base station modulation.

FIG. 52E illustrates EVM and Magnitude error vs shaped IQ input level using base station modulation.

FIG. 52F illustrates carrier feed thru vs. shaped IQ input signal level using base station modulation.

FIG. 52G illustrates Rho vs. LO signal level using base station modulation.

FIG. 52H illustrates transmitted channel power vs. LO signal level using base station modulation.

FIG. 52I illustrates ACPR vs. LO signal level using base station modulation.

FIG. 52J illustrates EVM and magnitude error vs LO signal level using base station modulation.

FIG. 52K illustrates carrier feed thru vs. LO signal level using base station modulation.

FIG. 52L illustrates carrier feed thru vs IQ input level over a wide range using base station modulation.

FIG. 52M illustrates ACPR vs. shaped IQ input signal level using base station modulation.

FIG. 52N illustrates Rho vs. shaped IQ input signal level using base station modulation.

FIG. 52O illustrates EVM, magnitude error, and phase error vs. shaped IQ input signal level using base station modulation.

FIG. 52P illustrates Rho vs. shaped IQ input signal level using mobile station modulation.

FIG. 52Q illustrates transmitted channel power vs. shaped IQ input signal level using mobile station modulation.

FIG. 52R illustrates ACPR vs. shaped IQ Input signal level using mobile station modulation.

FIG. 52S illustrates EVM, magnitude error, and phase error vs. shaped IQ input level using mobile station modulation.

FIG. 52T illustrates carrier feed thru vs. shaped I Q input signal level using mobile station modulation.

FIG. 52U illustrates Rho vs. LO signal level using mobile station modulation.

FIG. 52V illustrates transmitted channel power vs. LO signal level using mobile station modulation.

FIG. 52W illustrates ACPR vs. LO signal level using mobile station modulation.

FIG. 52X illustrates EVM and magnitude error vs. LO signal level using mobile station modulation.

FIG. 52Y illustrates carrier feed thru vs. LO signal level using mobile station modulation.

FIG. 52Z illustrates an approximate power budget for a CDMA modulator based on the modulator 2910.

Figures 52B-Z illustrate that the UFT-based complex modulator 2910 comfortably exceeds the IS-95 transmitter performance requirements for both mobile and base station modulations, even with signal level variations. Testing indicates that Rho as well as carrier feed through and ACPR are not overly sensitive to variations in I/Q levels and LO levels. Estimated power consumption for the modulator 2910 is lower than equivalent two-state superheterodyne architecture. This means that a

practical UFT based CDMA transmitter can be implemented in bulk CMOS and efficiently produced in volume.

The UFT architecture achieves the highest linearity per milliwatt of power consumed of any radio technology of which the inventors are aware. This efficiency comes without a performance penalty, and due to the inherent linearity of the UFT technology, several important performance parameters may actually be improved when compared to traditional transmitter techniques.

Since the UFT technology can be implemented in standard CMOS, new system partitioning options are available that have not existed before. As an example, since the entire UFT-based modulator can be implemented in CMOS, it is plausible that the modulator and other transmitter functions can be integrated with the digital baseband processor leaving only a few external components such as the final bandpass filter and the power amplifier. In addition to the UFT delivering the required linearity and dynamic range performance, the technology also has a high level of immunity to digital noise that would be found on the same substrate when integrated with other digital circuitry. This is a significant step towards enabling a complete wireless system-on-chip solution

It is noted that the test setup, procedures, and results discussed above and shown in the figures were provided for illustrative purposes only, and do not limit the invention to any particular embodiment, implementation or application.

8.0 *Integrated Up-conversion and Spreading of a Baseband Signal*

Previous sections focused on up-converting a spread spectrum signal directly from baseband-to-RF, without preforming any IF processing. In these embodiments, the baseband signal was already a spread spectrum signal prior to up-conversion. The following discussion focuses on embodiments that perform the spreading function and the frequency translation function in a simultaneously and in an integrated manner.

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One type of spreading code is Code Division Multiple Access (or CDMA), although the invention is not limited to this. The present invention can be implemented in CDMA, and other spread spectrum systems as will be understood by those skilled in the arts based on the teachings herein.

8.1 Integrated Up-Conversion and Spreading Using an Amplitude Shaper

FIG. 53A illustrates a spread spectrum transmitter 5300 that is based on the UFT-based modulator 2604 that was discussed in FIG. 26A. Spread spectrum transmitter 5300 performs simultaneous up-conversion and spreading of an input baseband signal 5302 to generate an output signal 5324. As will shown, the spreading is accomplished by placing the spreading code on the control signals that operate the UFT modules in the modulator 2604 so that the spreading and up-conversion are accomplished in an integrated manner. In order to limit sidelobe spectral growth in the output signal 5324, the amplitude of the input baseband signal 5302 is shaped so as to correspond with the spreading code. The operation of spread spectrum transmitter 5300 is described in detail as follows with reference to flowchart 6700 that is shown in FIG 67. The order of the steps in flowchart 6700 are not limiting and may be re-arranged as will be understood by those skilled in the arts. (This is generally true of all flowcharts discussed herein).

In step 6701, the spread spectrum transmitter 5300 receives the input baseband signal 5302.

In step 6702, the oscillator 2646 generates the clock signal 2645. As described earlier, the clock signal 2645 is in embodiments a sub-harmonic of the output signal 5324. Furthermore, in embodiments of the invention, the clock signal 2645 is a periodic square wave or sinusoidal clock signal.

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In step 6704, a spreading code generator 5314 generates a spreading code 5316. In embodiments of the invention, the spreading code 5316 is a PN code, or any other type of spreading code that is useful for generating spread spectrum signals.

In step 6706, the multiplier 5318 modulates the clock signal 2645 with the spreading code 5316 to generate spread clock signal 5320. As such, the spread clock signal 5320 carries the spreading code 5316.

In step 6708, the control signal generator 2642 receives the spread clock signal 5320, and generates control signals 5321 and 5322 that operate the UFT modules in the modulator 2604. The control signals 5321 and 5322 are similar to clock signals 2623 and 2627 that were discussed in FIG. 26. In other words, the clock signals 5321 and 5322 include a plurality of pulses having a pulse width T_A that is established to improve energy transfer to a desired harmonic in the resulting harmonically rich signal. Additionally, the control signals 5321 and 5322 are phase shifted with respect to each other by approximately 180 degrees (although the invention is not limited to this example), as were the control signals 2623 and 2627. However, the control signals 5321 and 5322 are modulated with (and carry) the spreading code 5316 because they were generated from spread clock signal 5320.

In step 6710, the amplitude shaper 5304 receives the input baseband signal 5302 and shapes the amplitude so that it corresponds with the spreading code 5316 that is generated by the code generator 5314, resulting in a shaped input signal 5306. This is achieved by feeding the spreading code 5316 back to the amplitude shaper 5304 and smoothing the amplitude of the input baseband signal 5302, accordingly.

FIG. 53B illustrates the resulting shaped input signal 5306 and the corresponding spreading code 5316. The amplitude of the input signal 5302 is shaped such that it is smooth and so that it has zero crossings that are in time synchronization with the spreading code 5316. By smoothing input signal amplitude, high frequency components are removed from the input signal prior to sampling, which results lower sidelobe energy in the harmonic images produced during sampling. Implementation

of amplitude shaper 5304 will be apparent to persons skilled in the art base on the functional teachings combined herein.

In step 6712, the low pass filter 5308 filters the shaped input signal 5306 to remove any unwanted high frequency components, resulting in a filtered signal 5310.

In step 6714, the modulator 2604 samples the signal 5310 in a balanced and differential manner according to the control signals 5320 and 5322, to generate a harmonically rich signal 5312. As discussed in reference to FIG. 26, the control signals 5320 and 5322 trigger the controlled switches in the modulator 2604, resulting in multiple harmonic images of the baseband signal 5302 in the harmonically rich signal 5312. Since the control signals carry the spreading code 5316, the modulator 2604 up-converts and spreads the filtered signal 5310 in an integrated manner during the sampling process. As such, the harmonic images in the harmonically rich signal 5312 are spread spectrum signals. FIG. 53C illustrates the harmonically rich signal 5312 that includes multiple harmonic images 5320a-n that repeat at harmonics of the sampling frequency $1/T_s$. Each image 5320a-n is a spread spectrum signal that contains the necessary amplitude and frequency information to reconstruct the input baseband signal 5302.

In step 6716, the optional filter 2606 selects a desired harmonic (or harmonics) from the harmonically rich signal 5312. This is presented by the passband 5322 selecting the spread harmonic 5320c in FIG. 53C.

In step 6718, the optional amplifier 2608 amplifies the desired harmonic (or harmonics) for transmission.

As mentioned above, an advantage of the spread spectrum transmitter 5300 is that the spreading and up-conversion is accomplished in a simultaneous and integrated manner. This is a result of modulating the control signals that operate the UFT modules in the balanced modulator 2604 with the spreading code prior to sampling of the baseband signal. Furthermore, by shaping the amplitude of the baseband signal prior to sampling, the sidelobe energy in the spread spectrum

1744.0450003

harmonics is minimized. As discussed above, minimal sidelobe energy is desirable in order to meet the sidelobe standards of the CDMA IS-95 standard (see FIGs. 43A and 43B).

FIG. 61 illustrates an IQ spread spectrum modulator 6100 that is based on the spread spectrum transmitter 5300. Spread spectrum modulator 6100 performs simultaneous up-conversion and spreading of an I baseband signal 6102 and a Q baseband signal 6118 to generate an output signal 6116 that carries both the I and Q baseband information. The operation of the modulator 6100 is described in detail with reference to the flowchart 6800 that is shown in FIGs. 68A and 68B. The steps in flowchart 6800 are not limiting and may be re-arranged as will be understood by those skilled in the arts.

In step 6801, the IQ modulator 6100 receives the I data signal 6102 and the Q data signal 6118.

In step 6802, the oscillator 2646 generates the clock signal 2645. As described earlier, the clock signal 2645 is in embodiments a sub-harmonic of the output signal 6116. Furthermore, in embodiments of the invention, the clock signal 2645 is a periodic square wave or sinusoidal clock signal.

In step 6804, an I spreading code generator 6140 generates an I spreading code 6144 for the I channel. Likewise, a Q spreading code generator 6138 generates a Q spreading code 6142 for the Q channel. In embodiments of the invention, the spreading codes are PN codes, or any other type of spreading code that is useful for generating spread spectrum signals. In embodiments of the invention, the I spreading code and Q spreading code can be the same spreading code. Alternatively, the I and Q spreading codes can be different to improve isolation between the I and Q channels, as will be understood by those skilled in the arts.

In step 6806, the multiplier 5318a modulates the clock signal 2645 with the I spreading code 6144 to generate a spread clock signal 6136. Likewise, the multiplier

5318b modulates the clock signal 2645 with the Q spreading code 6142 to generate a spread clock signal 6134.

In step 6808, the control signal generator 2642a receives the I clock signal 6136 and generates control signals 6130 and 6132 that operate the UFT modules in the modulator 2604a. The controls signals 6130 and 6132 are similar to clock signals 2623 and 2627 that were discussed in FIG. 26. The difference being that signals 6130 and 6132 are modulated with (and carry) the I spreading code 6144. Likewise, the control signal generator 2642b receives the Q clock signal 6134 and generates control signals 6126 and 6128 that operate the UFT modules in the modulator 2604b.

In step 6810, the amplitude shaper 5304a receives the I data signal 6102 and the shapes the amplitude so that it corresponds with the spreading code 6144, resulting in I shaped data signal 6104. This is achieved by feeding the spreading code 6144 back to the amplitude shaper 5304a.. The amplitude shaper then shapes the amplitude of the input baseband signal 6102 to correspond to the spreading code 6144, as described for spread spectrum transmitter 5300. More specifically, the amplitude of the input signal 6102 is shaped such that it is smooth and so that it has zero crossings that are in time synchronization with the I spreading code 6144. Likewise, the amplitude shaper 5304b receives the Q data signal 6118 and shapes amplitude of the Q data signal 6118 so that it corresponds with the Q spreading code 6142, resulting in Q shaped data signal 6120.

In step 6812, the low pass filter 5308a filters the I shaped data signal 6104 to remove any unwanted high frequency components, resulting in a I filtered signal 6106. Likewise, the low pass filter 5308b filters the Q shaped data signal 6120, resulting in Q filtered signal 6122.

In step 6814, the modulator 2604a samples the I filtered signal 6106 in a balanced and differential manner according to the control signals 6130 and 6132, to generate a harmonically rich signal 6108. As discussed in reference to FIG. 26, the control signals 6130 and 6132 trigger the controlled switches in the modulator 2604a,

resulting in multiple harmonic images in the harmonically rich signal 6108, where each image contains the I baseband information. Since the control signals 6130 and 6132 also carry the I spreading code 6144, the modulator 2604a up-converts and spreads the filtered signal 6106 in an integrated manner during the sampling process. As such, the harmonic images in the harmonically rich signal 6108 are spread spectrum signals.

In step 6816, the modulator 2604b samples the Q filtered signal 6122 in a balanced and differential manner according to the control signals 6126 and 6128, to generate a harmonically rich signal 6124. The control signals 6126 and 6128 trigger the controlled switches in the modulator 2604b, resulting in multiple harmonic images in the harmonically rich signal 6124, where each image contains the Q baseband information. As with modulator 2604a, the control signals 6126 and 6128 carry the Q spreading code 6142 so that the modulator 2604b up-converts and spreads the filtered signal 6122 in an integrated manner during the sampling process. In other words, the harmonic images in the harmonically rich signal 6124 are also spread spectrum signals.

In step 6818, a 90 signal combiner 6146 combines the I harmonically rich signal 6108 and the Q harmonically rich signal 6124, to generate the IQ harmonically rich signal 6148. The IQ harmonically rich signal 6148 contains multiple harmonic images, where each images contains the spread I data and the spread Q data. The 90 degree combiner phase shifts the Q signal 6124 relative to the I signal 6108 so that no increase in spectrum width is needed for the IQ signal 6148, when compared the I signal or the Q signal.

In step 6820, the optional bandpass filter 2606 select the harmonic (or harmonics) of interest from the harmonically rich signal 6148, to generate signal 6114.

In step 6222, the optional amplifier 2608 amplifies the desired harmonic 6114 for transmission.

1744.0450003

8.2 Integrated Up-Conversion and Spreading Using a Smoothing Varying Clock Signal

FIG. 54A illustrates a spread spectrum transmitter 5400 that is a second embodiment of balanced UFT modules that perform up-conversion and spreading simultaneously. More specifically, the spread spectrum transmitter 5400 does simultaneous up-conversion and spreading of an I data signal 5402a and a Q data signal 5402b to generate an IQ output signal 5428. Similar to modulator 6100, transmitter 5400 modulates the clock signal that controls the UFT modules with the spreading codes to spread the input I and Q signals during up-conversion. However, the transmitter 5400 modulates the clock signal by smoothly varying the instantaneous frequency or phase of a voltage controlled oscillator (VCO) with the spreading code. The transmitter 5400 is described in detail as follows with reference to a flowchart 6900 that is shown in FIGs. 69A and 69B.

In step 6901, the transmitter 5400 receives the I baseband signal 5402a and the Q baseband signal 5402b.

In step 6902, a code generator 5423 generates a spreading code 5422. In embodiments of the invention, the spreading code 5422 is a PN code or any other type off useful code for spread spectrum systems. Additionally, in embodiments of the invention, there are separate spreading codes for the I and Q channels.

In step 6904, a clock driver circuit 5421 generates a clock driver signal 5420 that is phase modulated according to a spreading code 5422. FIG. 54B illustrates the clock driver signal 5420 as series of pulses, where the instantaneous frequency (or phase) of the pulses is determined by the spreading code 5422, as shown. In embodiments of the invention, the phase of the pulses in the clock driver 5420 is varied smoothly in correlation with the spreading code 5422.

In step 6906, a voltage controlled oscillator 5418 generates a clock signal 5419 that has a frequency that varies according to a clock driver signal 5420. As

mentioned above, the phase of the pulses in the clock driver 5420 is varied smoothly in correlation with the spreading code 5422 in embodiments of the invention. Since the clock driver 5420 controls the oscillator 5418, the frequency of the clock signal 5419 varies smoothly as a function of the PN code 5422. By smoothly varying the frequency of the clock signal 5419, the sidelobe growth in the spread spectrum images is minimized during the sampling process.

In step 6908, the pulse generator 2644 generates a control signal 5415 based on the clock signal 5419 that is similar to either one the controls signals 2623 or 2627 (in FIGs. 27A and 27B). The control signal 5415 carries the spreading code 5422 via the clock signal 5419. In embodiments of the invention, the pulse width (T_A) of the control signal 5415 is established to enhance or optimize energy transfer to specific harmonics in the harmonically rich signal 5428 at the output. For the Q channel, a phase shifter 5414 shifts the phase of the control signal 5415 by 90 degrees to implement the desired quadrature phase shift between the I and Q channels, resulting in a control signal 5413.

In step 6910, a low pass filter (LPF) 5406a filters the I data signal 5402a to remove any unwanted high frequency components, resulting in an I signal 5407a. Likewise, a LPF 5406b filters the Q data signal 5402b to remove any unwanted high frequency components, to generate the Q signal 5407b.

In step 6912, a UFT module 5408a samples the I data signal 5407a according to the control signal 5415 to generate a harmonically rich signal 5409a. The harmonically rich signal 5409a contains multiple spread spectrum harmonic images that repeat at harmonics of the sampling frequency. Similar to transmitter 5300, the harmonic images in signal 5409a carry the I baseband information, and are spread spectrum due to the spreading code on the control signal 5415.

In step 6914, a UFT module 5408b samples the Q data signal 5407b according to the control signal 5413 to generate harmonically rich signal 5409b. The harmonically rich signal 5409b contains multiple spread spectrum harmonic images

that repeat at harmonics of the sampling frequency. The harmonic images in signal 5409a carry the Q baseband information, and are spread spectrum due to the spreading code on the control signal 5413.

In step 6916, a signal combiner 5410 combines the harmonically rich signal 5409a with the harmonically rich signal 5409b to generate an IQ harmonically rich signal 5412. The harmonically rich signal 5412 carries multiple harmonic images, where each image carries the spread I data and the spread Q data.

In step 6918, the optional bandpass filter 5424 selects a harmonic (or harmonics) of interest for transmission, to generate the IQ output signal 5428.

FIG. 54C illustrates a transmitter 5430 that is similar to the transmitter 5400 except that the UFT modules are replaced by balanced UFT modulators 2604 that were described in FIG. 26. Also, the pulse generator is replaced by the control signal generator 2642 to generate the necessary control signals to operate the UFT modules in the balanced modulators. By replacing the UFT modules with balanced UFT modulators, sidelobe suppression can be improved.

9.0   Shunt Receiver Embodiments Utilizing UFT Modules

In this section, example receiver embodiments are presented that utilize UFT modules in a differential and shunt configuration. More specifically, embodiments, according to the present invention, are provided for reducing or eliminating DC offset and/or reducing or eliminating circuit re-radiation in receivers, including I/Q modulation receivers and other modulation scheme receivers. These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained

herein. The invention is intended and adapted to include such alternate embodiments.

9.1 *Example I/Q Modulation Receiver Embodiments*

FIG. 70A illustrates an exemplary I/Q modulation receiver 7000, according to an embodiment of the present invention. I/Q modulation receiver 7000 has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation.

I/Q modulation receiver 7000 comprises a first UFD module 7002, a first optional filter 7004, a second UFD module 7006, a second optional filter 7008, a third UFD module 7010, a third optional filter 7012, a fourth UFD module 7014, a fourth filter 7016, an optional LNA 7018, a first differential amplifier 7020, a second differential amplifier 7022, and an antenna 7072.

I/Q modulation receiver 7000 receives, down-converts, and demodulates a I/Q modulated RF input signal 7082 to an I baseband output signal 7084, and a Q baseband output signal 7086. I/Q modulated RF input signal 7082 comprises a first information signal and a second information signal that are I/Q modulated onto an RF carrier signal. I baseband output signal 7084 comprises the first baseband information signal. Q baseband output signal 7086 comprises the second baseband information signal.

Antenna 7072 receives I/Q modulated RF input signal 7082. I/Q modulated RF input signal 7082 is output by antenna 7072 and received by optional LNA 7018. When present, LNA 7018 amplifies I/Q modulated RF input signal 7082, and outputs amplified I/Q signal 7088.

First UFD module 7002 receives amplified I/Q signal 7088. First UFD module 7002 down-converts the I-phase signal portion of amplified input I/Q signal 7088

according to an I control signal 7090. First UFD module 7002 outputs an I output signal 7098.

In an embodiment, first UFD module 7002 comprises a first storage module 7024, a first UFT module 7026, and a first voltage reference 7028. In an embodiment, a switch contained within first UFT module 7026 opens and closes as a function of I control signal 7090. As a result of the opening and closing of this switch, which respectively couples and de-couples first storage module 7024 to and from first voltage reference 7028, a down-converted signal, referred to as I output signal 7098, results. First voltage reference 7028 may be any reference voltage, and is preferably ground. I output signal 7098 is stored by first storage module 7024.

In an embodiment, first storage module 7024 comprises a first capacitor 7074. In addition to storing I output signal 7098, first capacitor 7074 reduces or prevents a DC offset voltage resulting from charge injection from appearing on I output signal 7098.

I output signal 7098 is received by optional first filter 7004. When present, first filter 7004 is in some embodiments a high pass filter to at least filter I output signal 7098 to remove any carrier signal "bleed through". In a preferred embodiment, when present, first filter 7004 comprises a first resistor 7030, a first filter capacitor 7032, and a first filter voltage reference 7034. Preferably, first resistor 7030 is coupled between I output signal 7098 and a filtered I output signal 7007, and first filter capacitor 7032 is coupled between filtered I output signal 7007 and first filter voltage reference 7034. Alternately, first filter 7004 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). First filter 7004 outputs filtered I output signal 7007.

Second UFD module 7006 receives amplified I/Q signal 7088. Second UFD module 7006 down-converts the inverted I-phase signal portion of amplified input I/Q signal 7088 according to an inverted I control signal 7092. Second UFD module 7006 outputs an inverted I output signal 7001.

1744.0450003

In an embodiment, second UFD module 7006 comprises a second storage module 7036, a second UFT module 7038, and a second voltage reference 7040. In an embodiment, a switch contained within second UFT module 7038 opens and closes as a function of inverted I control signal 7092. As a result of the opening and closing of this switch, which respectively couples and de-couples second storage module 7036 to and from second voltage reference 7040, a down-converted signal, referred to as inverted I output signal 7001, results. Second voltage reference 7040 may be any reference voltage, and is preferably ground. Inverted I output signal 7001 is stored by second storage module 7036.

In an embodiment, second storage module 7036 comprises a second capacitor 7076. In addition to storing inverted I output signal 7001, second capacitor 7076 reduces or prevents a DC offset voltage resulting from charge injection from appearing on inverted I output signal 7001.

Inverted I output signal 7001 is received by optional second filter 7008. When present, second filter 7008 is a high pass filter to at least filter inverted I output signal 7001 to remove any carrier signal "bleed through". In a preferred embodiment, when present, second filter 7008 comprises a second resistor 7042, a second filter capacitor 7044, and a second filter voltage reference 7046. Preferably, second resistor 7042 is coupled between inverted I output signal 7001 and a filtered inverted I output signal 7009, and second filter capacitor 7044 is coupled between filtered inverted I output signal 7009 and second filter voltage reference 7046. Alternately, second filter 7008 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Second filter 7008 outputs filtered inverted I output signal 7009.

First differential amplifier 7020 receives filtered I output signal 7007 at its non-inverting input and receives filtered inverted I output signal 7009 at its inverting input. First differential amplifier 7020 subtracts filtered inverted I output signal 7009 from filtered I output signal 7007, amplifies the result, and outputs I baseband output

signal 7084. Because filtered inverted I output signal 7009 is substantially equal to an inverted version of filtered I output signal 7007, I baseband output signal 7084 is substantially equal to filtered I output signal 7009, with its amplitude doubled. Furthermore, filtered I output signal 7007 and filtered inverted I output signal 7009 may comprise substantially equal noise and DC offset contributions from prior down-conversion circuitry, including first UFD module 7002 and second UFD module 7006, respectively. When first differential amplifier 7020 subtracts filtered inverted I output signal 7009 from filtered I output signal 7007, these noise and DC offset contributions substantially cancel each other.

Third UFD module 7010 receives amplified I/Q signal 7088. Third UFD module 7010 down-converts the Q-phase signal portion of amplified input I/Q signal 7088 according to an Q control signal 7094. Third UFD module 7010 outputs an Q output signal 7003.

In an embodiment, third UFD module 7010 comprises a third storage module 7048, a third UFT module 7050, and a third voltage reference 7052. In an embodiment, a switch contained within third UFT module 7050 opens and closes as a function of Q control signal 7094. As a result of the opening and closing of this switch, which respectively couples and de-couples third storage module 7048 to and from third voltage reference 7052, a down-converted signal, referred to as Q output signal 7003, results. Third voltage reference 7052 may be any reference voltage, and is preferably ground. Q output signal 7003 is stored by third storage module 7048.

In an embodiment, third storage module 7048 comprises a third capacitor 7078. In addition to storing Q output signal 7003, third capacitor 7078 reduces or prevents a DC offset voltage resulting from charge injection from appearing on Q output signal 7003.

Q output signal 7003 is received by optional third filter 7012. When present, in an embodiment, third filter 7012 is a high pass filter to at least filter Q output signal 7003 to remove any carrier signal "bleed through". In an embodiment, when present,

third filter 7012 comprises a third resistor 7054, a third filter capacitor 7056, and a third filter voltage reference 7058. Preferably, third resistor 7054 is coupled between Q output signal 7003 and a filtered Q output signal 7011, and third filter capacitor 7056 is coupled between filtered Q output signal 7011 and third filter voltage reference 7058. Alternately, third filter 7012 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Third filter 7012 outputs filtered Q output signal 7011.

Fourth UFD module 7014 receives amplified I/Q signal 7088. Fourth UFD module 7014 down-converts the inverted Q-phase signal portion of amplified input I/Q signal 7088 according to an inverted Q control signal 7096. Fourth UFD module 7014 outputs an inverted Q output signal 7005.

In an embodiment, fourth UFD module 7014 comprises a fourth storage module 7060, a fourth UFT module 7062, and a fourth voltage reference 7064. In an embodiment, a switch contained within fourth UFT module 7062 opens and closes as a function of inverted Q control signal 7096. As a result of the opening and closing of this switch, which respectively couples and de-couples fourth storage module 7060 to and from fourth voltage reference 7064, a down-converted signal, referred to as inverted Q output signal 7005, results. Fourth voltage reference 7064 may be any reference voltage, and is preferably ground. Inverted Q output signal 7005 is stored by fourth storage module 7060.

In an embodiment, fourth storage module 7060 comprises a fourth capacitor 7080. In addition to storing inverted Q output signal 7005, fourth capacitor 7080 reduces or prevents a DC offset voltage resulting from charge injection from appearing on inverted Q output signal 7005.

Inverted Q output signal 7005 is received by optional fourth filter 7016. When present, fourth filter 7016 is a high pass filter to at least filter inverted Q output signal 7005 to remove any carrier signal "bleed through". In a preferred embodiment, when present, fourth filter 7016 comprises a fourth resistor 7066, a fourth filter

capacitor 7068, and a fourth filter voltage reference 7070. Preferably, fourth resistor 7066 is coupled between inverted Q output signal 7005 and a filtered inverted Q output signal 7013, and fourth filter capacitor 7068 is coupled between filtered inverted Q output signal 7013 and fourth filter voltage reference 7070. Alternately, fourth filter 7016 may comprise any other applicable filter configuration as would be understood by persons skilled in the relevant art(s). Fourth filter 7016 outputs filtered inverted Q output signal 7013.

Second differential amplifier 7022 receives filtered Q output signal 7011 at its non-inverting input and receives filtered inverted Q output signal 7013 at its inverting input. Second differential amplifier 7022 subtracts filtered inverted Q output signal 7013 from filtered Q output signal 7011, amplifies the result, and outputs Q baseband output signal 7086. Because filtered inverted Q output signal 7013 is substantially equal to an inverted version of filtered Q output signal 7011, Q baseband output signal 7086 is substantially equal to filtered Q output signal 7013, with its amplitude doubled. Furthermore, filtered Q output signal 7011 and filtered inverted Q output signal 7013 may comprise substantially equal noise and DC offset contributions of the same polarity from prior down-conversion circuitry, including third UFD module 7010 and fourth UFD module 7014, respectively. When second differential amplifier 7022 subtracts filtered inverted Q output signal 7013 from filtered Q output signal 7011, these noise and DC offset contributions substantially cancel each other.

Additional embodiments relating to addressing DC offset and re-radiation concerns, applicable to the present invention, are described in co-pending Patent Application No.,"DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," Attorney Docket No. 1744.0880000, which is herein incorporated by reference in its entirety.

9..1.1 Example I/Q Modulation Control Signal Generator Embodiments

FIG. 70B illustrates an exemplary block diagram for I/Q modulation control signal generator 7023, according to an embodiment of the present invention. I/Q modulation control signal generator 7023 generates I control signal 7090, inverted I control signal 7092, Q control signal 7094, and inverted Q control signal 7096 used by I/Q modulation receiver 7000 of FIG. 70A. I control signal 7090 and inverted I control signal 7092 operate to down-convert the I-phase portion of an input I/Q modulated RF signal. Q control signal 7094 and inverted Q control signal 7096 act to down-convert the Q-phase portion of the input I/Q modulated RF signal. Furthermore, I/Q modulation control signal generator 7023 has the advantage of generating control signals in a manner such that resulting collective circuit re-radiation is radiated at one or more frequencies outside of the frequency range of interest. For instance, potential circuit re-radiation is radiated at a frequency substantially greater than that of the input RF carrier signal frequency.

I/Q modulation control signal generator 7023 comprises a local oscillator 7025, a first divide-by-two module 7027, a 180 degree phase shifter 7029, a second divide-by-two module 7031, a first pulse generator 7033, a second pulse generator 7035, a third pulse generator 7037, and a fourth pulse generator 7039.

Local oscillator 7025 outputs an oscillating signal 7015. FIG. 70C shows an exemplary oscillating signal 7015.

First divide-by-two module 7027 receives oscillating signal 7015, divides oscillating signal 7015 by two, and outputs a half frequency LO signal 7017 and a half frequency inverted LO signal 7041. FIG. 70C shows an exemplary half frequency LO signal 7017. Half frequency inverted LO signal 7041 is an inverted version of half frequency LO signal 7017. First divide-by-two module 7027 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

180 degree phase shifter 7029 receives oscillating signal 7015, shifts the phase of oscillating signal 7015 by 180 degrees, and outputs phase shifted LO signal 7019.

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180 degree phase shifter 7029 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s). In alternative embodiments, other amounts of phase shift may be used.

Second divide-by two module 7031 receives phase shifted LO signal 7019, divides phase shifted LO signal 7019 by two, and outputs a half frequency phase shifted LO signal 7021 and a half frequency inverted phase shifted LO signal 7043. FIG. 70C shows an exemplary half frequency phase shifted LO signal 7021. Half frequency inverted phase shifted LO signal 7043 is an inverted version of half frequency phase shifted LO signal 7021. Second divide-by-two module 7031 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

First pulse generator 7033 receives half frequency LO signal 7017, generates an output pulse whenever a rising edge is received on half frequency LO signal 7017, and outputs I control signal 7090. FIG. 70C shows an exemplary I control signal 7090.

Second pulse generator 7035 receives half frequency inverted LO signal 7041, generates an output pulse whenever a rising edge is received on half frequency inverted LO signal 7041, and outputs inverted I control signal 7092. FIG. 70C shows an exemplary inverted I control signal 7092.

Third pulse generator 7037 receives half frequency phase shifted LO signal 7021, generates an output pulse whenever a rising edge is received on half frequency phase shifted LO signal 7021, and outputs Q control signal 7094. FIG. 70C shows an exemplary Q control signal 7094.

Fourth pulse generator 7039 receives half frequency inverted phase shifted LO signal 7043, generates an output pulse whenever a rising edge is received on half frequency inverted phase shifted LO signal 7043, and outputs inverted Q control signal 7096. FIG. 70C shows an exemplary inverted Q control signal 7096.

1744.0450003

In an embodiment, control signals 7090, 7021, 7041 and 7043 include pulses having a width equal to one-half of a period of I/Q modulated RF input signal 7082. The invention, however, is not limited to these pulse widths, and control signals 7090, 7021, 7041, and 7043 may comprise pulse widths of any fraction of, or multiple and fraction of, a period of I/Q modulated RF input signal 7082.

First, second, third, and fourth pulse generators 7033, 7035, 7037, and 7039 may be implemented in circuit logic, hardware, software, or any combination thereof, as would be known by persons skilled in the relevant art(s).

As shown in FIG. 70C, in an embodiment, control signals 7090, 7021, 7041, and 7043 comprise pulses that are non-overlapping in other embodiments the pulses may overlap. Furthermore, in this example, pulses appear on these signals in the following order: I control signal 7090, Q control signal 7094, inverted I control signal 7092, and inverted Q control signal 7096. Potential circuit re-radiation from I/Q modulation receiver 7000 may comprise frequency components from a combination of these control signals.

For example, FIG. 70D shows an overlay of pulses from I control signal 7090, Q control signal 7094, inverted I control signal 7092, and inverted Q control signal 7096. When pulses from these control signals leak through first, second, third, and/or fourth UFD modules 7002, 7006, 7010, and 7014 to antenna 7072 (shown in FIG. 70A), they may be radiated from I/Q modulation receiver 7000, with a combined waveform that appears to have a primary frequency equal to four times the frequency of any single one of control signals 7090, 7021, 7041, and 7043. FIG. 70 shows an example combined control signal 7045.

FIG. 70D also shows an example I/Q modulation RF input signal 7082 overlaid upon control signals 7090, 7094, 7092, and 7096. As shown in FIG. 70D, pulses on I control signal 7090 overlay and act to down-convert a positive I-phase portion of I/Q modulation RF input signal 7082. Pulses on inverted I control signal 7092 overlay and act to down-convert a negative I-phase portion of I/Q modulation

1744.0450003

RF input signal 7082. Pulses on Q control signal 7094 overlay and act to down-convert a rising Q-phase portion of I/Q modulation RF input signal 7082. Pulses on inverted Q control signal 7096 overlay and act to down-convert a falling Q-phase portion of I/Q modulation RF input signal 7082.

As FIG. 70D further shows in this example, the frequency ratio between the combination of control signals 7090, 7021, 7041, and 7043 and I/Q modulation RF input signal 7082 is approximately 4:3. Because the frequency of the potentially re-radiated signal, i.e., combined control signal 7045, is substantially different from that of the signal being down-converted, i.e., I/Q modulation RF input signal 7082, it does not interfere with signal down-conversion as it is out of the frequency band of interest, and hence may be filtered out. In this manner, I/Q modulation receiver 7000 reduces problems due to circuit re-radiation. As will be understood by persons skilled in the relevant art(s) from the teachings herein, frequency ratios other than 4:3 may be implemented to achieve similar reduction of problems of circuit re-radiation.

It should be understood that the above control signal generator circuit example is provided for illustrative purposes only. The invention is not limited to these embodiments. Alternative embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) for I/Q modulation control signal generator 7023 will be apparent to persons skilled in the relevant art(s) from the teachings herein, and are within the scope of the present invention.

Additional embodiments relating to addressing DC offset and re-radiation concerns, applicable to the present invention, are described in co-pending patent application titled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," which is herein incorporated by reference in its entirety.

9.1.2 Detailed Example I/Q Modulation Receiver Embodiment with Exemplary Waveforms

1744.0450003

FIG. 70E illustrates a more detailed example circuit implementation of I/Q modulation receiver 7000, according to an embodiment of the present invention. FIGS. 70F-P show example waveforms related to an example implementation of I/Q modulation receiver 7000 of FIG. 70E.

FIGS. 70F and 70G show first and second input data signals 7047 and 7049 to be I/Q modulated with a RF carrier signal frequency as the I-phase and Q-phase information signals, respectively.

FIGS. 70I and 70J show the signals of FIG. 70F and 70G after modulation with a RF carrier signal frequency, respectively, as I-modulated signal 7051 and Q-modulated signal 7053.

FIG. 70H shows an I/Q modulation RF input signal 7082 formed from I-modulated signal 7051 and Q-modulated signal 7053 of FIGS. 70I and 70J, respectively.

FIG. 70O shows an overlaid view of filtered I output signal 7007 and filtered inverted I output signal 7009.

FIG. 70P shows an overlaid view of filtered Q output signal 7011 and filtered inverted Q output signal 7013.

FIGS. 70K and 70L show I baseband output signal 7084 and Q baseband output signal 7086, respectfully. A data transition 7055 is indicated in both I baseband output signal 7084 and Q baseband output signal 7086 The corresponding data transition 7055 is indicated in I-modulated signal 7051 of FIG. 70I, Q-modulated signal 7053 of FIG. 70J, and I/Q modulation RF input signal 7082 of FIG. 70H.

FIGS. 70M and 70N show I baseband output signal 7084 and Q baseband output signal 7086 over a wider time interval.

9.2   Example Single Channel Receiver Embodiment

FIG. 70Q illustrates an example single channel receiver 7091, corresponding to either the I or Q channel of I/Q modulation receiver 7000, according to an embodiment of the present invention. Single channel receiver 7091 can down-convert an input RF signal 7097 modulated according to AM, PM, FM, and other modulation schemes. Refer to section 7.4.1 above for further description on the operation of single channel receiver 7091.

9.3 Alternative Example I/Q Modulation Receiver Embodiment

FIG. 70R illustrates an exemplary I/Q modulation receiver 7089, according to an embodiment of the present invention. I/Q modulation receiver 7089 receives, down-converts, and demodulates an I/Q modulated RF input signal 7082 to an I baseband output signal 7084, and a Q baseband output signal 7086. I/Q modulation receiver 7089 has additional advantages of reducing or eliminating unwanted DC offsets and circuit re-radiation, in a similar fashion to that of I/Q modulation receiver 7000 described above.

10. Shunt Transceiver Embodiments Using UFT Modules

In this section, example transceiver embodiments are presented that utilize UFT modules in a shunt configuration for balanced up-conversion and balanced down-conversion. More specifically,

a signal channel transceiver embodiment is presented that incorporates the balanced transmitter 5600 (FIG. 56A) and the receiver 7091 (FIG. 70Q). Additionally, an IQ transceiver embodiment is presented that incorporate balanced IQ transmitter 5700 (FIG. 57) and IQ receiver 7000 (FIG. 70A).

These transceiver embodiments incorporate the advantages described above for the balanced transmitter 5600 and the balanced receiver 7091. More specifically, during

up-conversion, an input baseband signal is up-converted in a balanced and differential fashion, so as to minimize carrier insertion and unwanted spectral growth. Additionally, during down-conversion, an input RF input signal is down-converted so that DC offset and re-radiation is reduced or eliminated. Additionally, since both transmitter and receiver utilize UFT modules for frequency translation, integration and cost saving can be realized.

These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

FIG. 71 illustrates a transceiver 7100 according to embodiments of the present invention. Transceiver 7100 includes the single channel receiver 7091, the balanced transmitter 5600, a diplexer 7108, and an antenna 7112. Transceiver 7100 up-converts a baseband input signal 7110 using the balanced transmitter 5600 resulting in an output RF signal 7106 that is radiated by the antenna 7112. Additionally, the transceiver 7100 also down-converts a received RF input signal 7104 using the receiver 7091 to output baseband signal 7102. The diplexer 7108 separates the transmit signal 7106 from the receive signal 7104 so that the same antenna 7112 can be used for both transmit and receive operations. The operation of transmitter 5600 is described above in section 7.1.3, to which the reader is referred for greater detail.

During up-conversion, the transmitter 5600 shunts the input baseband signal 7110 to ground in a differential and balanced fashion according to the control signals 2623 and 2627, resulting in the harmonically rich signal 7114. The harmonically rich signal 7114 includes multiple harmonic images that repeat at harmonics of the sampling frequency of the control signals, where each harmonic image contains the necessary amplitude, frequency, and phase information to reconstruct the baseband

signal 7110. The optional filter 2606 can be included to select a desired harmonic from the harmonically rich signal 7114. The optional amplifier 2608 can be included to amplify the desired harmonic resulting in the output RF signal 7106, which is transmitted by antenna 7112 after the diplexer 7108. A detailed description of the transmitter 5600 is included in section 7.1.3, to which the reader is referred for further details.

During down-conversion, the receiver 7091 alternately shunts the received RF signal 7104 to ground according to control signals 7093 and 7095, resulting in the down-converted output signal 7102. A detailed description of receiver 7091 is included in sections 9.1 and 9.2, to which the reader is referred for further details.

FIG. 72 illustrates IQ transceiver 7200 according to embodiments of the present invention. IQ transceiver 7200 includes the IQ receiver 7000, the IQ transmitter 5700, a diplexer 7214, and an antenna 7216. Transceiver 7200 up-converts an I baseband signal 7206 and a Q baseband signal 7208 using the IQ transmitter 5700 (FIG. 57) to generate an IQ RF output signal 7212. A detailed description of the IQ transmitter 5700 is included in section 7.2.2, to which the reader is referred for further details. Additionally, the transceiver 7200 also down-converts a received RF signal 7210 using the IQ Receiver 7000, resulting in I baseband output signal 7202 and a Q baseband output signal 7204. A detailed description of the IQ receiver 7000 is included in section 9.1, to which the reader is referred for further details.

11. Conclusion

Example implementations of the methods, systems and components of the invention have been described herein. As noted elsewhere, these example implementations have been described for illustrative purposes only, and are not limiting. Other implementation embodiments are possible and covered by the

1744.0450003

invention, such as but not limited to software and software/hardware implementations of the systems and components of the invention. Such implementation embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

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While various application embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments.

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1744.0450003

What is Claimed Is:

1.   A method for up-converting a baseband signal, comprising the steps of:

         (1)   receiving the baseband signal; and

         (2)   differentially sampling the baseband signal according to a first control signal and a second control signal resulting in a plurality of harmonic images that are each representative of the baseband signal, wherein said first and second control signals have pulse widths that improve energy transfer to a desired harmonic image of said plurality of harmonics.

2.   The method of claim 1, further comprising the steps of:

         (3)   selecting said desired harmonic from said harmonic images that are generated in step (2); and

         (4)   transmitting said desired harmonic over a communications medium.

3.   The method of claim 1, further comprising the step of:

         (3)   minimizing DC offset voltages between sampling modules during step (2), and thereby minimizing carrier insertion in said harmonic images.

4.   The method of claim 3, wherein step (3) comprises the step of maintaining a reference voltage between said sampling modules during said differential sampling.

5.   The method of claim 1, wherein step (2) comprises the steps of:

         (a)   converting said baseband signal into a differential baseband signal having a first differential baseband component and a second differential baseband component;

         (b)   sampling said first differential component according to said first control signal to generate a first harmonically rich signal, and sampling said second

7 differential component according to said second control signal to generate a second

8 harmonically rich signal, wherein said second control signal is phase shifted relative

9 to said first control signal as measured by a master clock signal; and

10 (c) combining said first harmonically rich signal and said second

11 harmonically rich signal to generate said harmonic images.

1 6. The method of claim 5, further comprising the step of:

2 (d) adding a reference voltage to said first differential component and said

3 second differential component prior to step (b), and thereby minimizing any DC offset

4 voltages during sampling of said first differential baseband component and said second

5 differential baseband component.

1 7. The method of claim 5, wherein said step (b) of sampling comprises the steps

2 of:

3 (i) generating said first control signal comprising a first plurality of pulses

4 and said second control signal comprising a second plurality of pulses; and

5 (ii) operating a first switch according to said first control signal to

6 periodically sample said first differential baseband component, and operating a second

7 switch according to said second control signal to periodically sample said second

8 differential baseband signal.

1 8. The method of claim 7, wherein said step (i) comprises the step of widening

2 pulse widths of said first control signal and said second control signal by a non-

3 negligible amount that tends away from zero time duration to extend the time that said

4 first switch and said second switch is closed in step (ii), and thereby improving energy

5 transfer to said desired harmonic image.

1744.0450003

9.   The method of claim 8, wherein said step of widening pulse widths comprises the step of widening pulse widths for said first and second control signals to a non-zero fraction of a period of the desired harmonic of interest.

10.   The method of claim 8, wherein said step of widening pulse widths comprises the step of widening pulse widths for said first and second control signals to approximately one-half of a period of said desired harmonic of interest.

11.   The method of claim 1, wherein said first control signal and said second control signal have a period of T_S so that said harmonics images repeat at $1/T_S$ in frequency, and wherein said second control signal is phase-shifted relative to said first control signal by approximately 180 degrees.

12.   The method of claim 1, wherein said pulse widths of said first control signal and said second control signal are a non-zero fraction of a period of said desired harmonic of interest.

13.   The method of claim 1, wherein said pulse widths of said first control signal and said second control signal are approximately one-half of a period of said desired harmonic of interest, and thereby improve energy transfer to said desired harmonic of interest.

14.   The method of claim 1, wherein said pulse widths of said first control signal and said second control signal are approximately one-half of a period of said desired harmonic of interest, and thereby improve energy transfer to said desired harmonic of interest.

1744.0450003

1   15.   The method of claim 1, wherein said harmonic images have an amplitude that

2   is proportional to the following equation:

$$\text{Amp}_n = \left[\frac{4\sin\left(\dfrac{n\pi T_A}{T_s}\right) \cdot \sin\left(\dfrac{n\pi}{2}\right)}{n\pi} \right]$$

where: T_s = period of said first and second control signals

             T_A = pulse width of said first and second control signals

             n = harmonic number of said harmonic image whose amplitude is

    determined.

16.   The method of claim 1, wherein said harmonic images have an amplitude that

is based on $n*(T_A/T_S)$, where T_S is a period of said first and second control signals,

T_A is a pulse width of pulses in said first and second control signals, and n is a

harmonic number of said harmonic image.

17.   A method for up-converting a baseband signal, comprising the steps of:

      (1)   receiving the baseband signal; and

      (2)   differentially sampling the baseband signal according to a first control

signal and a second control signal resulting in a plurality of harmonic images that are

each representative of the baseband signal, wherein said first and second control

6 signals have pulse widths that are a non-negligible fraction of a period associated with a desired harmonic image.

1 18. The method of claim 17, wherein said pulse width are each approximately ½
2 a period associated with said desired harmonic, and thereby shifting energy into said
3 desired harmonic.

4 19. The method of claim 17, further comprising the step of:
5 (3) minimizing DC offset voltages between sampling modules during said
6 step (2), and thereby minimizing carrier insertion in said harmonic images.

1 20. The method of claim 19, wherein step (3) comprises the step of maintaining
2 a reference voltage between said sampling modules during said differential sampling.

1 21. The method of claim 17, wherein step (2) comprises the steps of:
2 (a) converting said baseband signal into a differential baseband signal
3 having a first differential baseband component and a second differential baseband
4 component;
5 (b) sampling said first differential component according to said first
6 control signal to generate a first harmonically rich signal, and sampling said second
7 differential component according to said second control signal to generate a second
8 harmonically rich signal, wherein said second control signal is phase shifted relative
9 to said first control signal; and
10 (c) combining said first harmonically rich signal and said second
11 harmonically rich signal to generate said harmonic images.

1 22 A method of up-converting a baseband signal, comprising the steps of:
2 (1) receiving a baseband signal and an inverted baseband signal;

1744.0450003

3   (2)   sampling the baseband signal according to a first control signal to

4   generate a first harmonically rich signal;

5   (3)   sampling said inverted baseband signal according to said second

6   control signal to generate a second harmonically rich signal, wherein said second

7   control signal is phase shifted relative to said first control signal;

8   (4)   combining said first harmonically rich signal and said second

9   harmonically rich signal to generate a third harmonically rich signal having harmonic

10   images that are representative of said baseband signal; and

11   wherein pulse widths of said first control signal and said second control signal

12   operate to improve energy transfer to a desired harmonic image in said third

13   harmonically rich signal.

1   23.   The method of claim 22, further comprising the step of:

2   (5)   band-pass filtering the desired harmonic.

3   24.   The method of claim 23, further comprising the step of transmitting said

4   filtered harmonic over a communications medium.

1   25.   The method of claim 22, further comprising the step of:

2   (5)   minimizing DC offset voltages between controlled switches that

3   perform said steps (2) and (3).

1   26.   The method of claim 25, wherein step (5) comprises the step of coupling said

2   controlled switches to a common reference voltage.

1   27   The method of claim 26, wherein step (5) comprises the step of coupling an

2   input and an output of said controlled switches to said common reference voltage.

1   28.   The method of claim 22, wherein said pulses of said first control signal and

2   said second control signal are each a non-negligible fraction of a period of said desired

3   harmonic.

1   29.   The method of claim 22, wherein said pulses of said first control signal and

2   said second control signal are each approximately one-half of a period of said desired

3   harmonic.

1   30.   The method of claim 22, wherein said pulses of said first and second control

2   signals have a pulse width of T_A, and wherein an amplitude of said harmonics in said

3   third harmonically rich signal are based on $n*(T_A/T_S)$, where T_S is a period of said first

4   and second control signal, and n is a harmonic number of said harmonic.

1   31.   The method of claim 22, wherein said pulses of said first and second control

2   signals have a pulse width of T_A, and wherein an amplitude of said harmonics in said

3   third harmonically rich signal are represented by the following equation:

$$Amp_n = \left[\frac{4\sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right]$$

4

5   wherein: T_S = period of said first and second control signals;

6   T_A = pulse width of said first and second control signals; and

7   n = harmonic number of said harmonic image whose amplitude is

8   determined.

1744 0450003

1 32.   The method of claim 22, wherein said step (2) of sampling comprises the steps
2   of:
3   (a)   receiving said baseband signal at a first port of a switch; and
4   (b)   operating said switch according to pulse widths T_A of said first control
5 signal to transfer non-negligible amounts energy to a second port of said switch
6 during said pulse widths T_A.

1 33.   The method of claim 22, wherein said step (3) of sampling comprises the steps
2 of:
3   (a)   receiving said inverted baseband signal at a first port of a switch; and
4   (b)   closing said switch during pulse widths T_A of said second control
5 signal to transfer non-negligible amounts energy to a second port of said switch.

1 34.   The method of claim 22, further comprising the step of amplifying said desired
2 harmonic image.

1 35.   The method of claim 22, further comprising the step of:
2   (5)   adding a voltage offset between controlled switches that perform said
3 sampling in steps (2) and steps (3), thereby causing carrier insertion in said harmonic
4 images that comprise said harmonically rich signal.

1 36.   The method of claim 22, wherein step (2) comprises the step of shunting the
2 baseband signal to ground according to said first control signal.

1 37.   The method of claim 34, wherein step (3) comprises the step of shunting the
2 inverted baseband signal to ground according to said second control signal.

1   38.   A method of up-converting a baseband signal, comprising the steps of:

2   (1)   receiving a baseband signal and an inverted baseband signal;

3   (2)   adding a common reference voltage to the baseband signal and the

4 inverted baseband signal, to generate a first combined signal and a second combined

5 signal, respectively;

6   (2)   sampling said first combined signal according to a first control signal

7 to generate a first harmonically rich signal;

8   (3)   sampling said second combined signal according to said second control

9 signal to generate a second harmonically rich signal, wherein said second control

10 signal is phase shifted approximately 180 degrees relative to said first control signal;

11   (4)   combining said first harmonically rich signal and said second

12 harmonically rich signal to generate a third harmonically rich signal having harmonic

13 images that are representative of said baseband signal;

14   wherein said pulses of said first and second control signals have a pulse width

15 of T_A, and wherein an amplitude of said harmonics in said third harmonically rich

16 signal are based on $n*(T_A/T_S)$, where T_S is a period of said first and second control

17 signal, and n is a harmonic number of said harmonic; and

18   wherein T_A established to improve energy transfer to a desired harmonic image

19 in said third harmonically rich signal.

1   39.   The method of claim 38, wherein said pulses of said first control signal and

2 said second control signal are a non-negligible fraction of a period of said desired

3 harmonic.

1   40.   The method of claim 38, wherein said pulses of said first control signal and

2 said second control signal are approximately one-half of a period of said desired

3 harmonic.

1744.0450003

41. The method of claim 38, wherein said pulses of said first and second control signals have a pulse width of T_A, and wherein an amplitude of said harmonics in said third harmonically rich signal are represented by the following equation:

$$Amp_n = \left[\frac{4\sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right]$$

wherein: T_S = period of said first and second control signals;

T_A = pulse width of said first and second control signals; and

n = harmonic number of said harmonic image whose amplitude is determined.

42. A method of up-converting a baseband signal, comprising the steps of:

(1) receiving a baseband signal and an inverted baseband signal;

(2) adding a common reference voltage to the baseband signal and the inverted baseband signal, to generate a first combined signal and a second combined signal, respectively;

(2) shunting said first combined signal to ground according to a first control signal to generate a first harmonically rich signal;

(3) shunting said second combined signal to ground according to said second control signal to generate a second harmonically rich signal, wherein said second control signal is phase shifted approximately 180 degrees relative to said first control signal so that second combined signal is not shunted to ground simultaneous with said first combined signal;

(4) combining said first harmonically rich signal and said second harmonically rich signal to generate a third harmonically rich signal having harmonic images that are representative of said baseband signal;

wherein said pulses of said first and second control signals have a pulse width of T_A, and wherein an amplitude of said harmonics in said third harmonically rich signal are based on $n*(T_A/T_S)$, where T_S is a period of said first and second control signal, and n is a harmonic number of said harmonic; and

wherein pulse widths of said first control signal and said second control signal are established to improve energy transfer to a desired harmonic image in said third harmonically rich signal.

43. The method of claim 42, wherein said pulses of said first control signal and said second control signal are a non-negligible fraction of a period of said desired harmonic.

44. The method of claim 42, wherein said pulses of said first control signal and said second control signal are approximately one-half of a period of said desired harmonic.

45. The method of claim 42, wherein said pulses of said first and second control signals have a pulse width of T_A, and wherein an amplitude of said harmonics in said third harmonically rich signal are represented by the following equation:

$$Amp_n = \left[\frac{4\sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right]$$

1744.0450003

wherein: T_S = period of said first and second control signals;

T_A = pulse width of said first and second control signals; and

n= harmonic number of said harmonic image whose amplitude is determined.

46.   A method of transmitting an IQ signal, the method comprising the steps:

(1)   receiving an I baseband signal and a Q baseband signal;

(2)   differentially sampling the I baseband signal according to a first control signal and a second control signal, to generate an I harmonically rich signal;

(3)   differentially sampling the Q baseband signal according to said first control signal and said second control signal, to generate a Q harmonically rich signal;

(4)   combining said I harmonically rich signal and said Q harmonically rich signal, to generate a IQ harmonically rich signal, said IQ harmonically rich signal having multiple harmonic images that contain information for reconstruction of the I and Q baseband signals; and

wherein said first and second control signals have pulse widths established to improve energy transfer to a desired harmonic image in said I and Q baseband signals.

47.   The method of claim 46, further comprising the steps of:

(5)   minimizing DC offset voltages between sampling modules during said sampling in step (2) and step (3).

48.   The method of claim 47, wherein step (5) comprises the step of coupling said sampling modules to a common reference voltage.

49.   The method of claim 47, wherein step (5) comprises the step of coupling said sampling modules to ground.

1744.0450003

1   50.   The method of claim 46, further comprising the step of:

2   (5)   selecting said desired harmonic from said harmonically rich signal.

1   51.   The method of claim 50, further comprising the step of:

2   (6)   transmitting said desired harmonic over a communications medium.

1   52.   The method of claim 46, wherein said pulses of said first control signal and

2   said second control signal are a non-negligible fraction of a period of said desired

3   harmonic.

1   53.   The method of claim 46, wherein said pulses of said first control signal and

2   said second control signal are approximately one-half a period of said desired

3   harmonic.

1   54.   The method of claim 46, wherein said pulses of said first and second control

2   signals have a pulse width of T_A, and wherein an amplitude of said harmonics in said

3   IQ harmonically rich signal are based on $n*(T_A/T_S)$, where T_S is a period of said first

4   and second control signal, and n is a harmonic number of said harmonic.

1   55.   The method of claim 46, wherein an amplitude of said harmonics is

2   represented by the following equation:

3

4

$$Amp_n = \left[\frac{4\sin\left(\dfrac{n\pi T_A}{T_s}\right) \cdot \sin\left(\dfrac{n\pi}{2}\right)}{n\pi} \right]$$

wherein: T_S = period of said first and second control signals;

T_A = pulse width of said first and second control signals; and

n= harmonic number of said harmonic image whose amplitude is determined.

56.   The method of claim 46, wherein step (2) comprises the steps of:

(a)   inverting the I baseband signal, resulting in an inverted I baseband signal;

(b)   sampling the I baseband signal according to the first control signal, and sampling said inverted I baseband signal according to said second control signal, wherein said second control signal is approximately 180 degree out-of-phase with respect said first control signal.

57.   The method of claim 56, further comprising the step of combining a reference voltage with said I baseband signal and said inverted I baseband signal prior to said step of sampling.

58.   The method of claim 56, wherein said step (b) comprises the steps of:

(i)   operating a first switch that samples said I baseband signal according to said first control signal; and

(ii)   operating a second switch that samples said inverted I baseband signal according to said second control signal.

59.   The method of claim 46, wherein step (3) comprises the steps of:

(a)   inverting the Q baseband signal, resulting in an inverted Q baseband signal;

(b)   sampling the Q baseband signal according to the first control signal, and sampling said inverted Q baseband signal according to said second control signal,

1   wherein said second control signal is approximately 180 degree out-of-phase with

2   respect said first control signal.

1   60.   The method of claim 59, further comprising the step of combining a reference

2   voltage with said Q baseband signal and said inverted Q baseband signal prior to said

3   step of sampling.

1   61.   The method of claim 59, wherein said step (b) comprises the steps of:

2   (i)   operating a first switch that samples said Q baseband signal according

3   to said first control signal; and

4   (ii)   operating a second switch that samples said inverted Q baseband signal

5   according to said second control signal.

1   62.   The method of claim 46, wherein step (2) comprises the steps of:

2   (a)   inverting the I baseband signal, resulting in an inverted I baseband

3   signal;

4   (b)   shunting the I baseband signal to ground according to the first control

5   signal, and shunting the inverted I baseband signal to ground according to said second

6   control signal, wherein said second control signal is approximately 180 degree out-

7   of-phase with respect said first control signal.

1   63.   The method of claim 46, wherein step (3) comprises the steps of:

2   (a)   inverting the Q baseband signal, resulting in an inverted I baseband

3   signal;

4   (b)   shunting the Q baseband signal to ground according to the first control

5   signal, and shunting the inverted Q baseband signal to ground according to said

6   second control signal, wherein said second control signal is approximately 180 degree

7   out-of-phase with respect said first control signal.

64. The method of claim 46, further comprising the step of:

(5) generating said first control signal and said second control signal, comprising the steps of:

(a) receiving a master clock signal having a frequency $(1/T_s)$ that is a sub-harmonic of said desired frequency;

(b) generating pulses in said first control signal to correspond with rising edges of said master clock signal; and

(c) generating pulses in said second control signal to correspond with falling edges of said master clock signal.

65. The method of claim 64, wherein said pulses in said first control signal and said second control signal have a pulse width T_A that are established to improve energy transfer to said desired harmonic in said IQ harmonically rich signal.

66. The method of claim 65, wherein said pulse width T_A is a non-negligible fraction of a period associated with said desired harmonic in said IQ harmonically rich signal.

67. A method of transmitting an IQ signal, the method comprising the steps:

(1) receiving an I baseband signal and a Q baseband signal;

(2) inverting said I baseband signal and said Q baseband signal, resulting in an inverted I baseband signal and an inverted Q baseband signal, respectively;

(3) summing a reference voltage with said I baseband signal and said inverted I baseband signal, resulting in a first I combined signal and a second I combined signal, respectively;

8   (4)   summing said reference voltage with said Q baseband signal and said

9   inverted Q baseband signal, resulting in a first Q combined signal and a second Q

10   combined signal, respectively;

11   (5)   sampling said first I combined signal according to a first control signal,

12   and sampling said second I combined signal according to said second control signal,

13   resulting in a first and second harmonically rich signals, respectively;

14   (6)   sampling said first Q combined signal according to a first control

15   signal, and sampling said second Q combined signal according to said second control

16   signal, resulting in a first and second Q harmonically rich signals, respectively;

17   (7)   combining said first I harmonically rich signal and said second I

18   harmonically rich signal to generate a third I harmonically rich signal, said third I

19   harmonically rich signal having multiple harmonic images that are each representative

20   of the I baseband signal;

21   (8)   combining said first Q harmonically rich signal and said second Q

22   harmonically rich signal to generate a third Q harmonically rich signal, said third Q

23   harmonically rich signal having multiple harmonic images that are each representative

24   of the Q baseband signal;

25   (9)   combining said third I harmonically rich signal and said third Q

26   harmonically rich signal to generate an IQ harmonically rich signal, said IQ

27   harmonically rich signal having multiple harmonic images that are each representative

28   of said I baseband signal and said Q baseband signal; and

29   wherein said harmonic images in said IQ harmonically rich signal repeat at a

30   multiple of $1/T_S$, where T_S is a period associated with said first control signal and said

31   second control signal.

1   68.   The method of claim 67, wherein step (9) comprises the steps of phase shifting

2   said third Q harmonically rich signal relative to said third I harmonically rich signal.

1   69.   The method of claim 67, wherein said second control signal is phase shifted

2   relative to said first control signal.

1   70.   The method of claim 67, wherein said second control signal is phase shifted

2   approximately 180 degrees relative to said first control signal.

1   71.   The method of claim 67, wherein said first control signal and said second

2   control signal have pulse widths T_A that is established to improve energy transfer to

3   a desired harmonic image in said IQ harmonically rich signal.

1   72.   The method of claim 71, wherein said pulse widths T_A are approximately one-

2   half of a period associated with said desired harmonic.

1   73.   The method of claim 71, wherein an amplitude of said harmonic images in said

2   IQ harmonically rich signal are based on $n*(T_A/T_S)$, where n is a harmonic number of

3   said harmonic image.

1   74.   The method of claim 71, wherein an amplitude of said harmonic images is

2   represented by the following equation:

3

$$Amp_n = \left[\frac{4\sin\left(\frac{n\pi T_A}{T_s}\right) \cdot \sin\left(\frac{n\pi}{2}\right)}{n\pi} \right]$$

4   wherein: T_S = period of said first and second control signals;

5   T_A = pulse width of said first and second control signals; and

1744.0450003

6   n= harmonic number of said harmonic image whose amplitude is

7   determined.

1   75.   A system for up-converting a baseband signal, comprising.

2   means for inverting said baseband signal, resulting in an inverted baseband

3 signal;

4   first sampling means for sampling said baseband signal according to a first

5 control signal, resulting in a first harmonically rich signal;

6   second sampling means for sampling said inverted baseband signal according

7 to a second control signal, resulting in a second harmonically rich signal;

8   means for combining said first harmonically rich signal and said second

9 harmonically rich signal, resulting in a third harmonically rich signal, wherein said

10 third harmonically rich signal contains multiple harmonic images that are each

11 representative of said baseband signal;

12   wherein said first and second control signals have a period of T_S so that said

13 harmonic images repeat at multiples of $1/T_S$;

14   wherein said second control signal is phase shifted relative to said first control

15 signal; and

16   wherein said first and second control signal comprise pulses having an

17 associated pulse width T_A that operates to improve energy transfer to a desired

18 harmonic image in said harmonically rich signal.

1   76.   The system of claim 75, wherein said pulse width T_A is approximately one-half

2 a period associated with said desired harmonic.

1   77.   The method of claim 75, wherein an amplitude of said harmonic images is

2   represented by the following equation:

$$\text{Amp}_n = \left[\frac{4\sin\left(\dfrac{n\pi T_A}{T_s}\right) \cdot \sin\left(\dfrac{n\pi}{2}\right)}{n\pi} \right]$$

3

wherein: T_S = period of said first and second control signals;

T_A = pulse width of said first and second control signals; and

n = harmonic number of said harmonic image whose amplitude is determined.

78.   The system of claim 75, further comprising:

means for limiting offset voltages between said first sampling means and said second sampling means.

79.   The system of claim 78, wherein said means for limiting comprises a means for distributing a reference voltage to said first sampling means and said second sampling means.

80.   The system of claim 79, wherein said means for distributing comprises a means for summing said reference with said baseband signal and said inverted baseband signal.

81.   The system of claim 75, further comprising a means for selecting said desired harmonic from said third harmonically rich signal.

82.   The system of claim 75, wherein said first sampling means comprises a means for shunting said baseband signal to ground according to said first control signal, and

3   wherein said second sampling means comprises a means for shunting said inverted

4   baseband signal to ground, according to said second control signal.

1   83.   A system of transmitting an IQ signal, the method comprising the steps:

2   (1)   means for receiving an I baseband signal and a Q baseband signal;

3   (2)   first differential sampling means for sampling the I baseband signal

4   according to a first control signal and a second control signal, to generate an I

5   harmonically rich signal, wherein said second control signal is phase shifted relative

6   to said first control signal;

7   (3)   second differential sampling means for sampling the Q baseband signal

8   according to said first control signal and said second control signal, to generate a Q

9   harmonically rich signal;

10   (4)   means for combining said I harmonically rich signal and said Q

11   harmonically rich signal, to generate an IQ harmonically rich signal, said IQ

12   harmonically rich signal having multiple harmonic images that contain amplitude and

13   frequency information for reconstruction of the I and Q baseband signals;

14   wherein said first and second control signals have a period of T_S so that said

15   harmonic images repeat at multiples of $1/T_S$; and

16   wherein said first and second control signal comprise pulses having an

17   associated pulse width T_A that operates to improve energy transfer to a desired

18   harmonic image in said harmonically rich signal.

1   84.   The system of claim 83, wherein said T_A is approximately one-half a period

2   of said desired harmonic.

1   85.   An apparatus for transmitting a baseband signal, said apparatus comprising:

2   a buffer/inverter, for receiving said baseband signal and generating an inverted

3   baseband signal;

4   a terminal for receiving a reference voltage;

5   a first summer, coupled to a first output of said buffer/inverter and said

6   terminal, said first summer summing said reference voltage with said baseband signal

7   and resulting in a first combined signal;

8   a second summer, coupled to a second output of said buffer inverter and said

9   terminal, said second summer summing said reference voltage with said inverted

10   baseband signal and resulting in a second combined signal;

11   a first controlled switch, coupled to an output of said first summer, said first

12   controlled switch sampling said first combined signal according to a first control

13   signal, and resulting in a first harmonically rich signal;

14   a second controlled switch, coupled to an output of said second summer, said

15   second controlled switch sampling said second combined signal according to a second

16   control signal, and resulting in a second harmonically rich signal;

17   a combiner, coupled to an output of said first controlled switch and an output

18   of said second controlled switch, said combiner combining said first harmonically rich

19   signal and said second harmonically rich signal, resulting in an third harmonically rich

20   signal;

21   wherein said first control signal and said second control signal comprises

22   pulses having a pulse width T_A that operates to improve energy transfer to a desired

23   harmonic is said third harmonically rich signal; and

24   wherein said first control signal and said second control signal are phase

25   shifted with respect to each other.

1   86.   The apparatus of claim 85, further comprising an inductor coupled between

2   said terminal and said outputs of said first and second controlled switches, and thereby

3   distributing said reference voltage to said outputs of said controlled switches.

1   87.   The apparatus of claim 86, wherein:

2   said first controlled switch comprises a first field effect transistor (FET), a

3   gate of said first FET coupled to said first control signal, a source of said first FET

4   receiving said first combined signal, and a drain of said first FET outputting said first

5   harmonically rich signal;

6   said second controlled switch comprises a second field effect transistor (FET),

7   a gate of said second FET coupled to said second control signal, a source of said

8   second FET receiving said second combined signal, and a drain of said second FET

9   outputting said second harmonically rich signal.

1   88.   The apparatus of claim 87, wherein said first FET conducts according to said

2   pulses of said first control signal, and said second FET conducts according to said

3   pulses of said second control signal.

1   89.   The apparatus of claim 87, wherein said pulse width T_A associated with said

2   first and second control signal is a non-negligible fraction of a period associated with

3   a desired harmonic in said third harmonically rich signal.

1   90.   The apparatus of claim 89, wherein said pulse width T_A is approximately one-

2   half a period of said desired harmonic image.

1   91.   The apparatus of claim 85, further comprising a bandpass filter coupled to an

2   output of said combiner to select said desired harmonic from said harmonically rich

3   signal.

1   92.   An apparatus for transmitting a baseband signal, said apparatus comprising:

2   a buffer/inverter, for receiving said baseband signal and generating an inverted

3   baseband signal;

4   a first controlled switch, coupled to an output of said buffer/inverter, said first

5   controlled switch shunting said baseband signal to ground according to a first control

6   signal, and resulting in a first harmonically rich signal;

7   a second controlled switch, coupled to a second output of said buffer/inverter,

8   said second controlled switch shunting said inverted baseband signal to ground

9   according to a second control signal, and resulting in a second harmonically rich

10   signal;

11   a combiner, coupled to an output of said first controlled switch and an output

12   of said second controlled switch, said combiner combining said first harmonically rich

13   signal and said second harmonically rich signal, resulting in an third harmonically rich

14   signal;

15   wherein said first control signal and said second control signal comprises

16   pulses having a pulse width T_A that operate to improve energy transfer to a desired

17   harmonic is said third harmonically rich signal; and

18   wherein said first control signal and said second control signal are phase

   shifted with respect to each other.

1   93.   The apparatus of claim 92, wherein:

2   said first controlled switch comprises a first field effect transistor (FET), a

3   gate of said first FET coupled to said first control signal, a source of said first FET

4   receiving said baseband signal and outputting said first harmonically rich signal, and

5   a drain of said first FET coupled to ground; and

6   said second controlled switch comprises a second field effect transistor (FET),

7   a gate of said second FET coupled to said second control signal, a source of said

8   second FET receiving said inverted baseband signal and outputting said second

9   harmonically rich signal, and a drain of said second FET coupled to ground.

1744.0450003

1 94.   The apparatus of claim 93, wherein said first FET and said second FET
2 alternately shunt said baseband signal and said inverted baseband signal to ground,
3 respectively, according to said first control signal and said second control signal, to
4 generate said harmonically rich signals.

1 95.   The apparatus of claim 92, wherein said pulse width T_A is approximately one-
2 half of a period associated with said desired harmonic in said third harmonically rich
3 signal.

Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal

Abstract

A balanced transmitter up-converts a baseband signal directly from baseband-to-RF. The up-conversion process is sufficiently linear that no IF processing is required, even in communications applications that have stringent requirements on spectral growth. In operation, the balanced modulator sub-harmonically samples the baseband signal in a balanced and differential manner, resulting in harmonically rich signal. The harmonically rich signal contains multiple harmonic images that repeat at multiples of the sampling frequency, where each harmonic contains the necessary information to reconstruct the baseband signal. The differential sampling is performed according to a first and second control signals that are phase shifted with respect to each other. In embodiments of the invention, the control signals have pulse widths (or apertures) that operate to improve energy transfer to a desired harmonic in the harmonically rich signal. A bandpass filter can then be utilized to select the desired harmonic of interest from the harmonically rich signal. The sampling modules that perform the sampling can be configured in either a series or a shunt configuration. In embodiments of the invention, DC offset voltages are minimized between the sampling modules to minimize or prevent carrier insertion into the harmonic images.

A274-19 wpd

1744.0450003

102

Universal Frequency
Translation (UFT)
module

Port 1

Port 2

Port 3

Control
Signal

FIG. 1A

Universal Frequency
Translation (UFT)
module 103

106

Port 1

Port 2

Port 3

Control Signal 108

FIG. 1B

Universal frequency
Down-conversion
(UFD) module 114

UFT module

Port 1

Port 2

115

Port 3

Control
Signal

FIG. 1C

Universal
Frequency Up-Conversion (UFU)
module 116

UFT module

Port 1

Port 2

117

Port 3

Control Signal

FIG. 10

Universal Frequency
Translation (UFT)
module 202

Port 1

Port 2/3

204

Control
Signal

Port 3

206

FIG. 2A

Port 2

208

S   D
              210
        G

Port 1

Port 3

control
signal

Fig. 2B

Universal Frequency
Up-Conversion (UFU) module 300
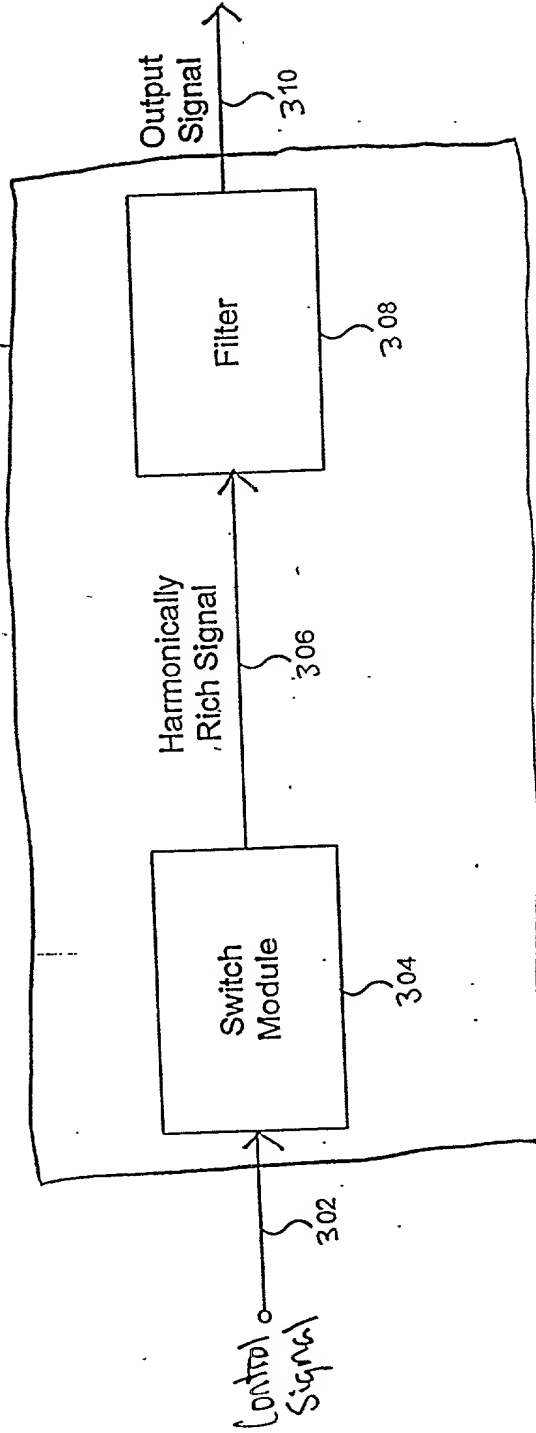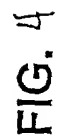
Control
Signal o——~——
302

Switch
Module
304

Harmonically
Rich Signal
~306

Filter
308

Output
Signal
~310

FIG. 3

Universal Frequency
Up-conversion (UFU) module 401

Output Signal

310

306

412

410

414

FUNC
308

Bias Signal

404

Port 1

402

405

Switch

UFT 450

Port
2

406

408

Control Signal

302

Port 3

switch module 304

FIG. 4

Universal Frequency
up-conversion
(UFU) Module 590

Unshaped Input
Signal

501

Pulse
Shaping
Module
(optional)

502

Control
Signal

302

Switch
Module

304

306

Filter

308

Output
Signal

310

FIG. 5

FIG. 6A

FIG. 6B
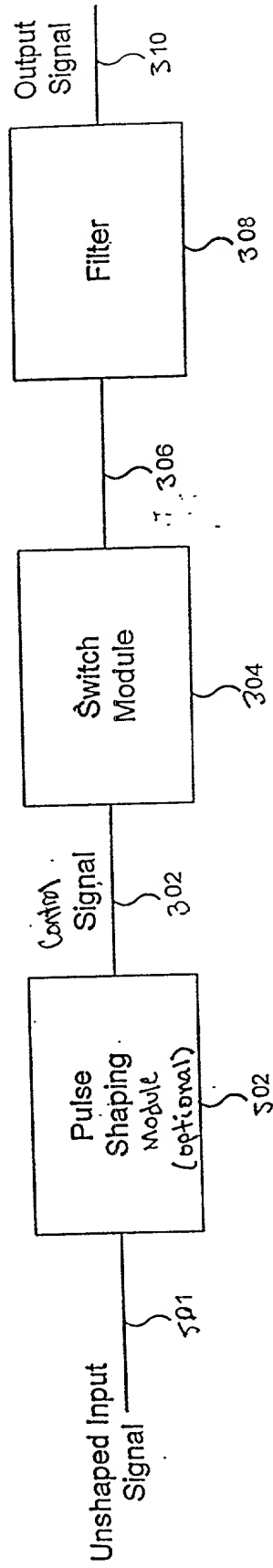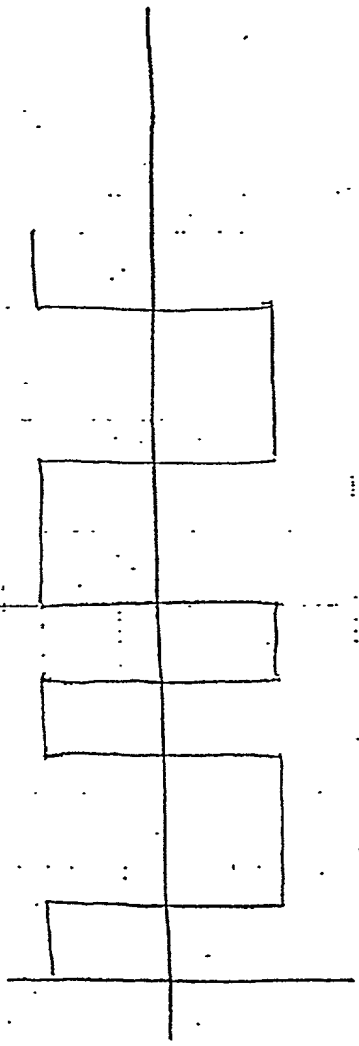
FIG. 6C

FIG. 6D

INFORMATION
SIGNAL
602
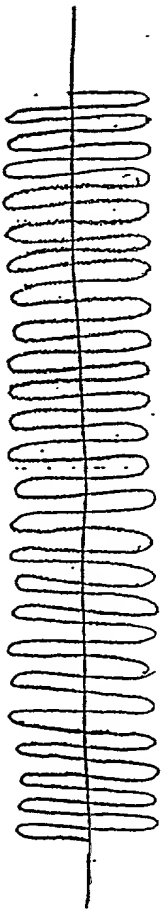
OSCILLATING
SIGNAL
604
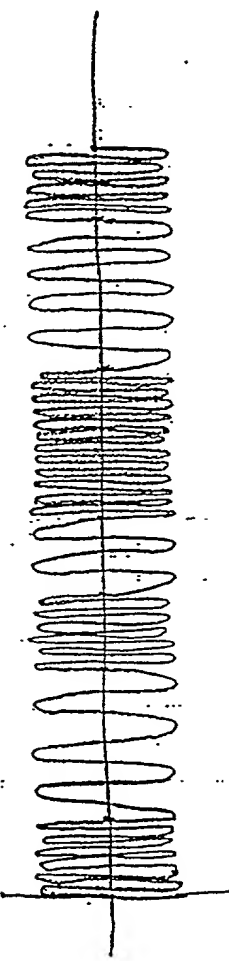
FREQUENCY MODULATED
INPUT SIGNAL
606

HARMONICALLY
RICH SIGNAL
(SHOWN AS SQUARE WAVE)
608

SEE FIG. 6E

FIG. 6

EXPANDED VIEW OF HARMONICALLY RICH SIGNAL 608

610   612

SEE FIG. 6F   SEE FIG. 6G

FIG. 6E

HARMONICS OF SIGNAL 610 (SHOWN SEPARATELY)

FUNDAMENTAL FREQUENCY 610A

THIRD HARMONIC 610B

FIFTH HARMONIC 610C

FIG. 6F

HARMONICS OF SIGNAL 612 (SHOWN SEPARATELY)

FUNDAMENTAL FREQUENCY 612A

THIRD HARMONIC 612B

FIFTH HARMONIC 612C

FIG. 6G

FIG. 6 (cont)

HARMONICS OF
SIGNALS 610 AND
612 (SHOWN
SIMULTANEOUSLY BUT
NOT SUMMED)

610

612

FILTERED
OUTPUT
SIGNAL

614

FIG 6H

FIG. 6I

FIG 6 (cont)

Receiver 702

Down-Conversion
Module 704

UFT   Module
706

FIG. 7

Transmitter 802

Up-conversion
Module 804

UFT Module
└ 806

FIG. 8

902

90b

Transmitter

Receiver

904

FIG. 9

Transceiver 1002

Transmitter 1004

| VFT Module | 1006 |

Receiver 1008

| UFT Module | 1010 |

FIG. 10

Transceiver 1102

Transmitter 1104

UFT Module

1106

Receiver 1108

FIG. 11

Transmitter 1202

ESR module (Transmit)
1204

Frequency
Up-conversion
Module

1206

1208

Receiver 1210

ESR module (Receive)
1212

Frequency
Down-conversion
module

1214

FIG. 12

Unified Down-Converting
and Filtering (UDF) module 1302

Frequency Down-Conversion
module
1304

Filtering
module
1306

UFT
Module

1308

FIG. 13

Receiver 1402

Unified Down-Converting
and Filtering
(UDF) module

1404

FIG. 14

Filter 1502 → Down-converter 1504 ⤳ Unified Down-Converting and Filtering (UDF) module 1506

FIG. 15A

Down-Converter 1508 → Filter 1510 ⤳ UDF module 1512

FIG. 15B

Filter 1514 → Down-Converter 1516 → Filter 1518 ⤳ UDF module 1520

FIG. 15C

Filter 1522 ⤳ UDF module 1524

FIG. 15D

Down-converter 1526 ⤳ UDF Module 1528

FIG. 15E

1530

Amplifier $\rightarrow$

1532

UOF Module

FIG. 15F

FIG. 16

Input
Signal
1704

Apparent
Input Filter

Frequency
Translator

Output
Signal
1710

1706

1708

FIG. 17

1802

Time / Node	t-1 (rising edge of ϕ_1)	t-1 (rising edge of ϕ_2)	t (rising edge of ϕ_1)	t (rising edge of ϕ_2)	t+1 (rising edge of ϕ_1)
1902	VI_{t-1} 1804	VI_{t-1} 1808	VI_t 1816	VI_t 1826	VI_{t+1} 1838
1904	—	VI_{t-1} 1810	VI_{t-1} 1818	VI_t 1828	VI_t 1840
1906	VO_{t-1} 1806	VO_{t-1} 1812	VO_t 1820	VO_t 1830	VO_{t+1} 1842
1908	—	VO_{t-1} 1814	VO_{t-1} 1822	VO_t 1832	VO_t 1844
1910	— 1807	—	VO_{t-1} 1824	VO_{t-1} 1834	VO_t 1846
1912	—	— 1815	—	VO_{t-1} 1836	VO_{t-1} 1848
1918	—	—	—	—	VI_t – 1850 $0.1 * VO_t$ $0.8 * VO_{t-1}$

FIG. 18

FIG. 19

ALIASING
MODULE

2000

DOWN-CONVERTED
OUTPUT SIGNAL

2012

2002

2016

INPUT
SIGNAL

2004

2008

2006

CONTROL
SIGNAL

FIG. 20A

ALIASING
MODULE

2000

INPUT
SIGNAL

2004

2010

2002

2008

CONTROL
SIGNAL

2006

DOWN-CONVERTED
OUPUT SIGNAL

2012

FIG. 20A-1

2014

FIG. 20B

t_0 t_1 t_2 t_3 t_4

2016

2022

FIG. 20C

t_0

2018   2020

FIG. 20D

t_0 2022   2024

FIG. 20E

2026

FIG. 20F

M

MODULATING baseband Signal 2102

2104

Transmitter

transmitted redundant spectrums 2106a-n

2108

Communications Medium

received redundant spectrums 2110a-n

2112

Receiver

demodulated baseband Signal 2114

FIG. 21

Fig. 22A

Amplitude

2201

2202

Time

Fig. 22B

Amplitude

2203

2204

Frequency

Fig. 22C

Amplitude

2205

2206b

$f_1 - f_2$

2206c

f_1

2206d

$f_1 + f_2$

Frequency

Fig. 22D

Amplitude

2205

2208c

$f_1 - f_2$

2209

2208d

f_1

$f_1 + f_2$

Frequency

FIG. 22E

Amplitude

2205

2210a — (f_1-f_2)

2210b — f_1

2211

2210d — (f_1+f_2)

Frequency

FIG. 22F

Amplitude

2212

Time

FIG. 23A

Fig. 13b

Amplitude

1205

1206a (f₁ - nf₂)
1206b f₁ - f₂
1206c f₁
1206d f₁ + f₂
1206n f₁ + nf₂

Frequency

Fig. 13c

Amplitude

1205

1206b
1206c
1206d
1207

Frequency

FIG. 23D

FIG. 23E

Amplitude

2205

$2208a$ $f_1 - nf_2$

$2208b$ $f_1 - 2f_2$

$2208c$ $f_1 - f_2$

2209

f_1

$2208d$ $f_1 + f_2$

$2208e$ $f_1 + 2f_2$

$2208n$ $f_1 + nf_2$

Frequency

FIG. 23F

Amplitude

2205

$2208c$

2209

$2208d$

2325

FIG. 24A

FIG. 24B.

Amplitude

2205

2210b
$(f_1 - f_2)$

2210c
2211
f_1

2210d
$(f_1 + f_2)$

Frequency

FIG. 24C.

Amplitude

2405

2406a
f_{IFA}

2406b
f_{IFB}

2407

2406c
f_{IFC}

Frequency

FIG. 24D

Amplitude

2406a

F_{IFA}

2205

Frequency

FIG. 24E

Amplitude

2406b

2407

F_{IFB}

2205

Frequency

FIG. 24F

Amplitude

2406c

2205

Frequency

FIG. 24G

Amplitude

2418a

Time

FIG. 24H

Amplitude

2418b

Time

FIG. 24I

Amplitude

2418c

Time

Amplitude

2212

Time

FIG. 24J

Fig. 25A

Fig. 25B

FIG. 26A

Amplitude

2610

2652a

1/Ts

2652b

2/Ts

2652c

3/Ts

2652n

n/Ts

Frequency

2630

FIG. 26B

Amplitude

2610

|1/Ts   2/Ts   3/1Ts   n/Ts   Frequency

2654a   2654b   2654c   2654n

2656

2633, 2638

FIG. 26C

FIG. 26D

FIG.27A

T_s

← 2645

FIG.27B

T_A

← 2623

FIG.27C

T_A

← 2627

FIG.27D

t_0 t_1

2702

← 2610

t_1

t_0

+1
−1

2704

← 2614

FIG.27E

+1
−1

2706

← 2616

t_1'

FIG.27F

FIG.27G V_R
2613

2709

2708

← 2630

t_1

FIG.27H V_R
2613

2711

2710

t_1

FIG.27I V_R
2613

2709a   2709b

2711a   2711b

2712

t_1

← 2634

T_A

2714

← 2633

Aperture = 500ps
Fundamental Clock = 200Mhz (5th Subharmonic)

Square Wave Frequency = 200Mhz

729mV

500mV

250mV

0V

0Hz   0.50GHz   1.00GHz   1.50GHz   1.87GHz

Frequency

2720a
2718a
2718b
2720b
2718c
2718d
2720c
2718e
2718f
2720d
2718g
2718h
2720e
2718i

☑ V
☐ V(Square_Wave)

FIG. 27J

FIG. 28A

FIG. 28B

FIG. 29

Fig. 30A

Fig. 30B

Fig. 30C
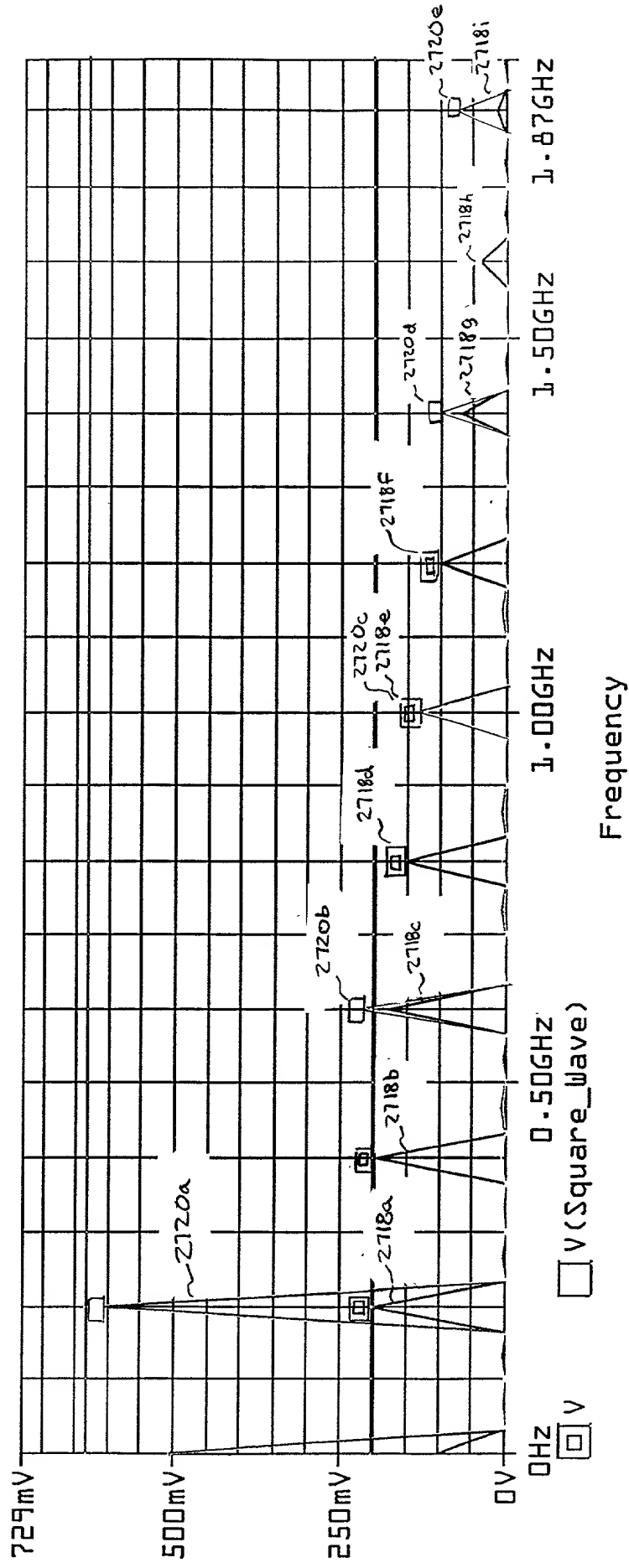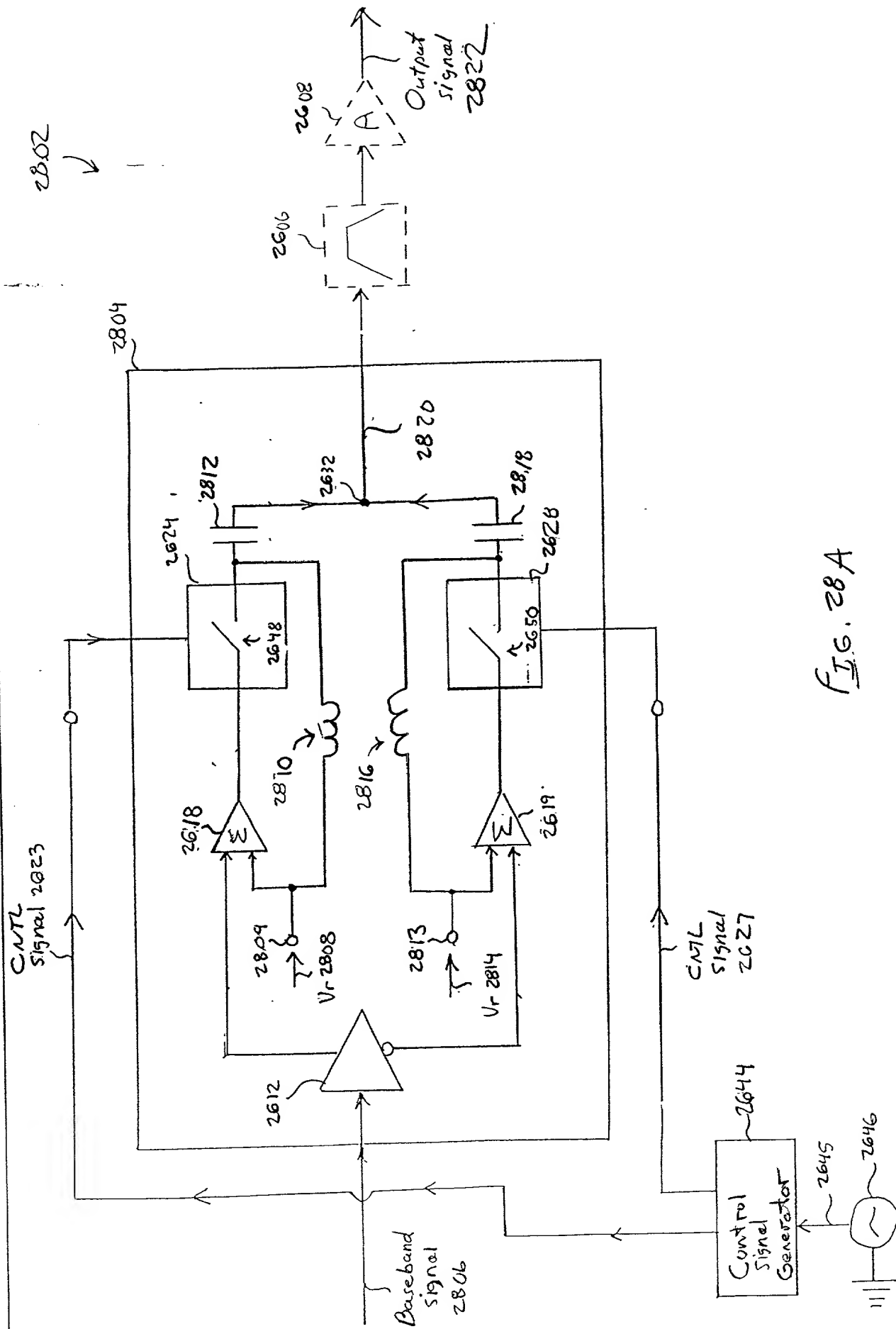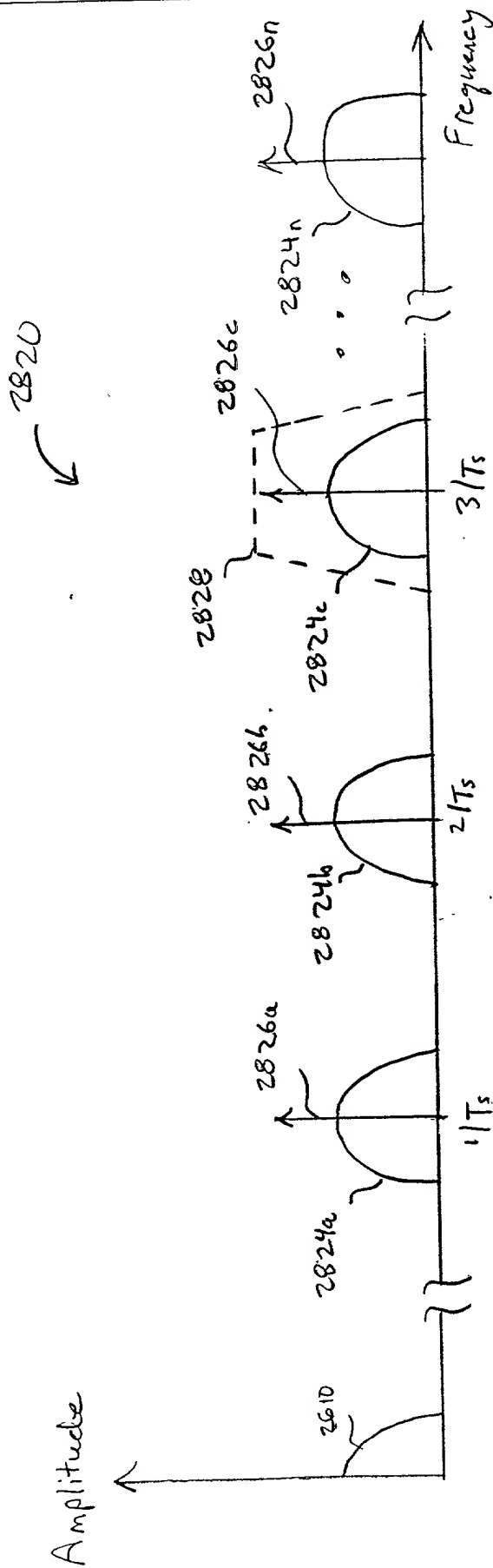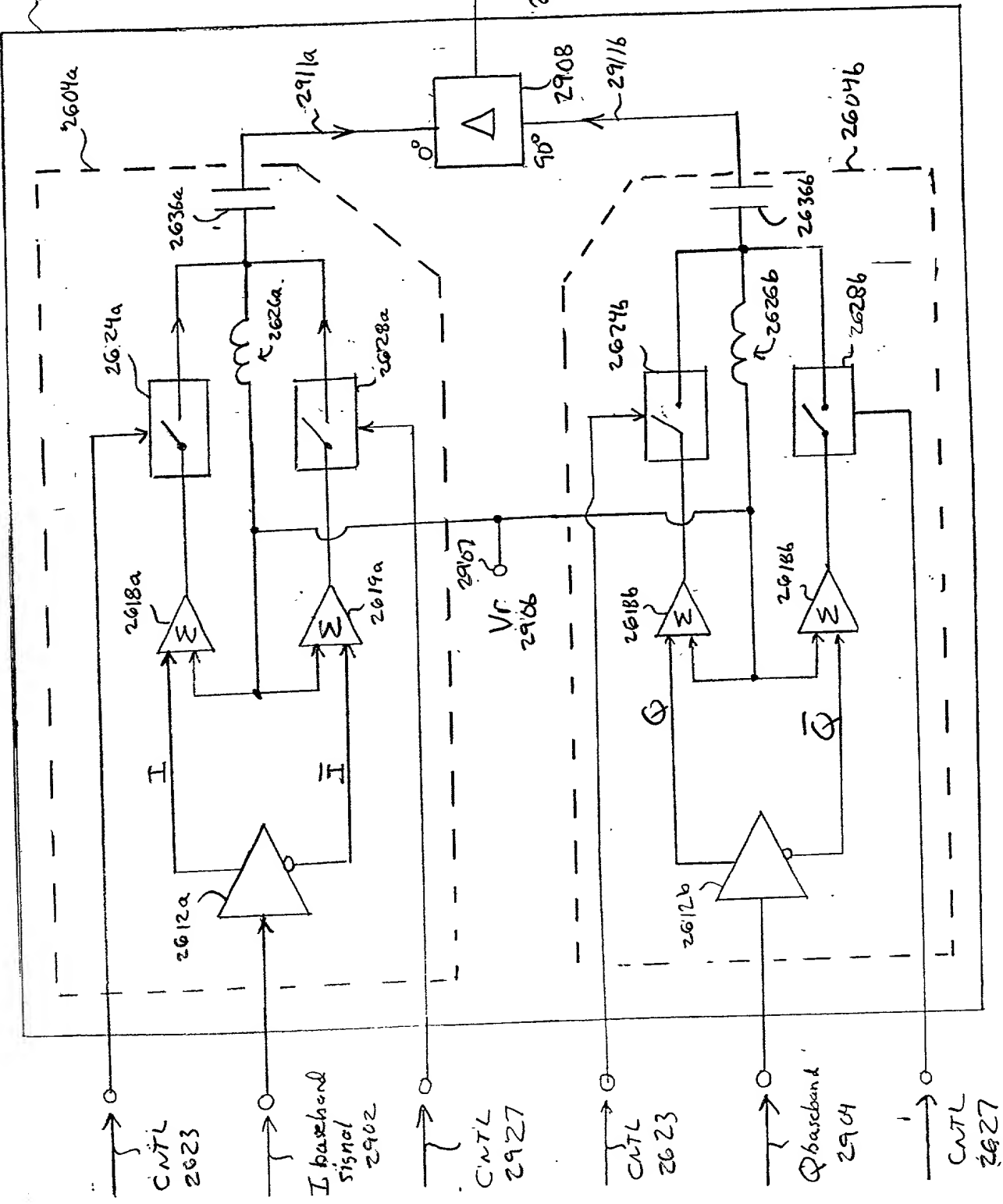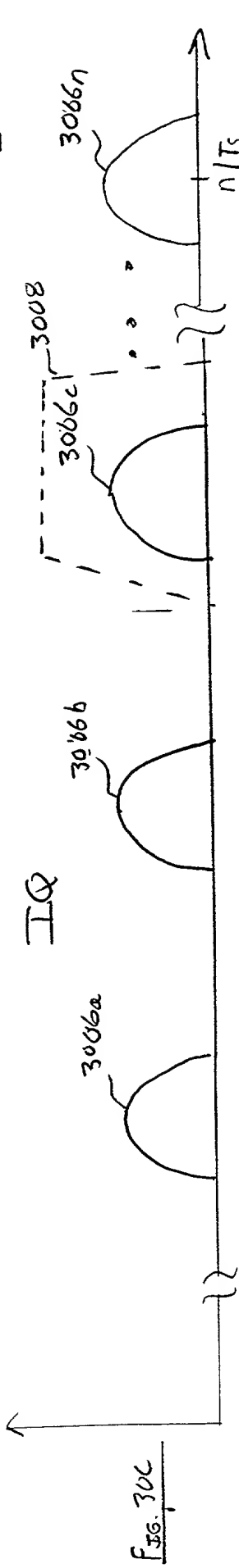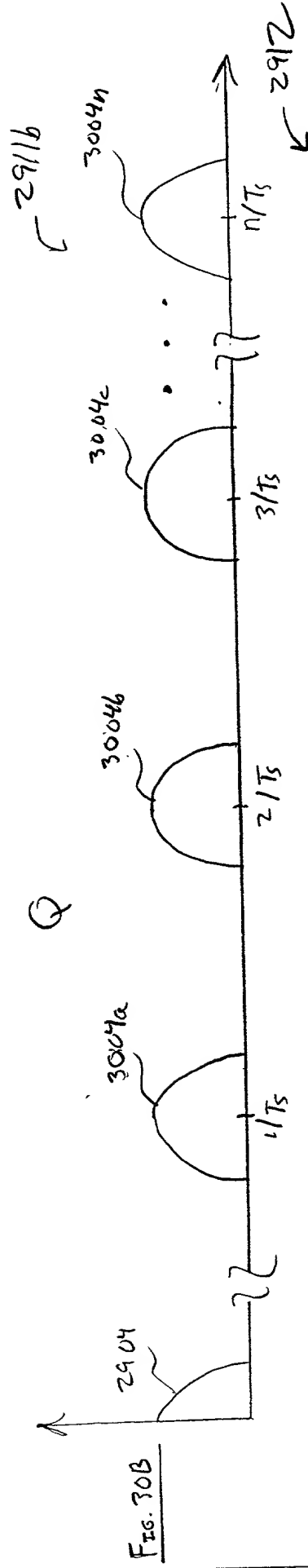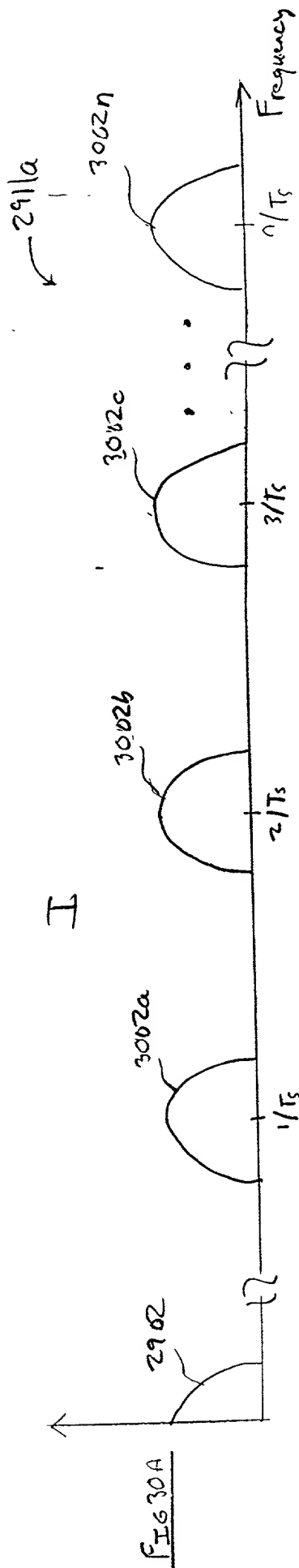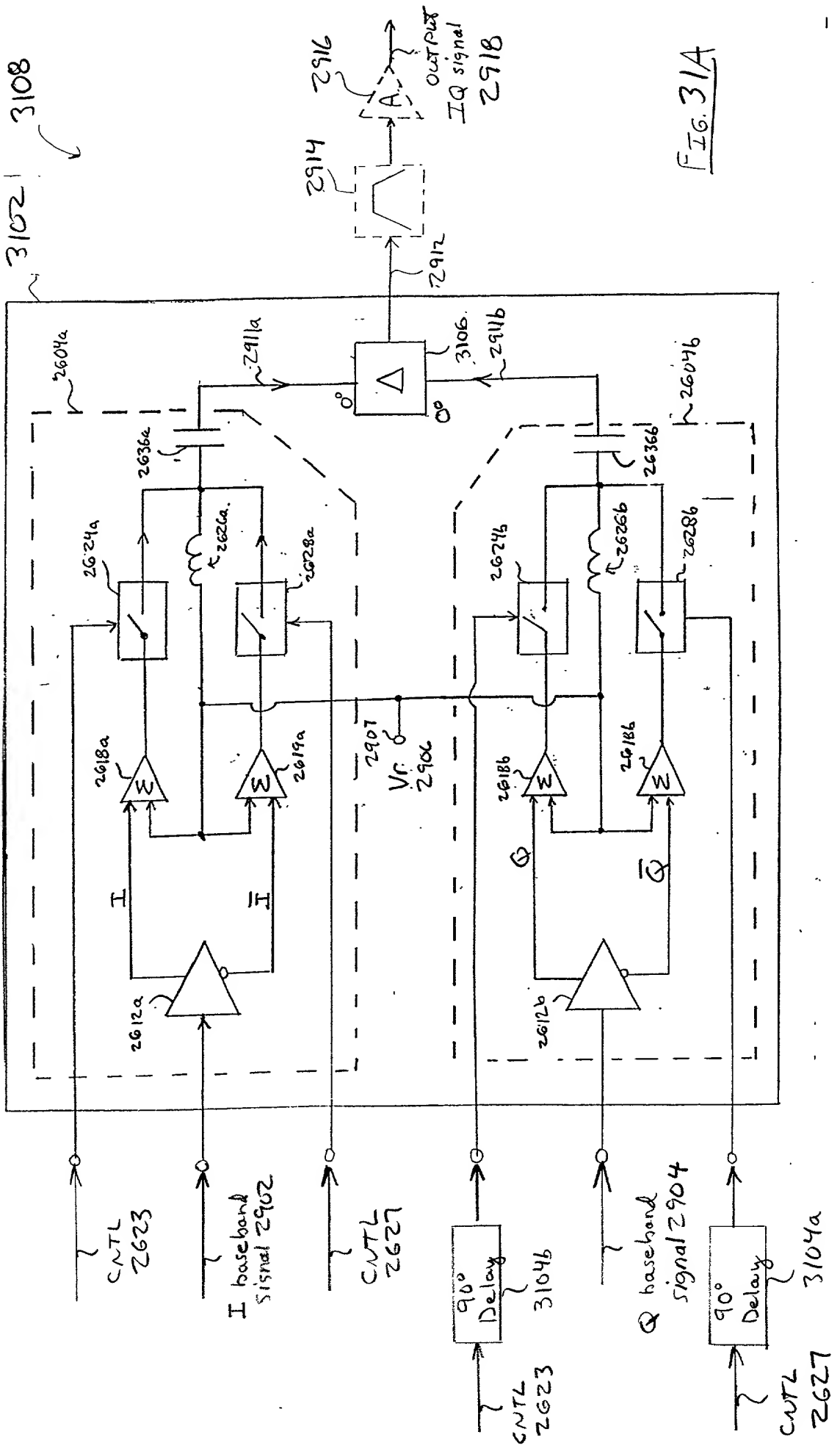
FIG. 31A

FIG. 31B

FIG. 32

FIG. 33

FIG. 34A

FIG. 34B

2920
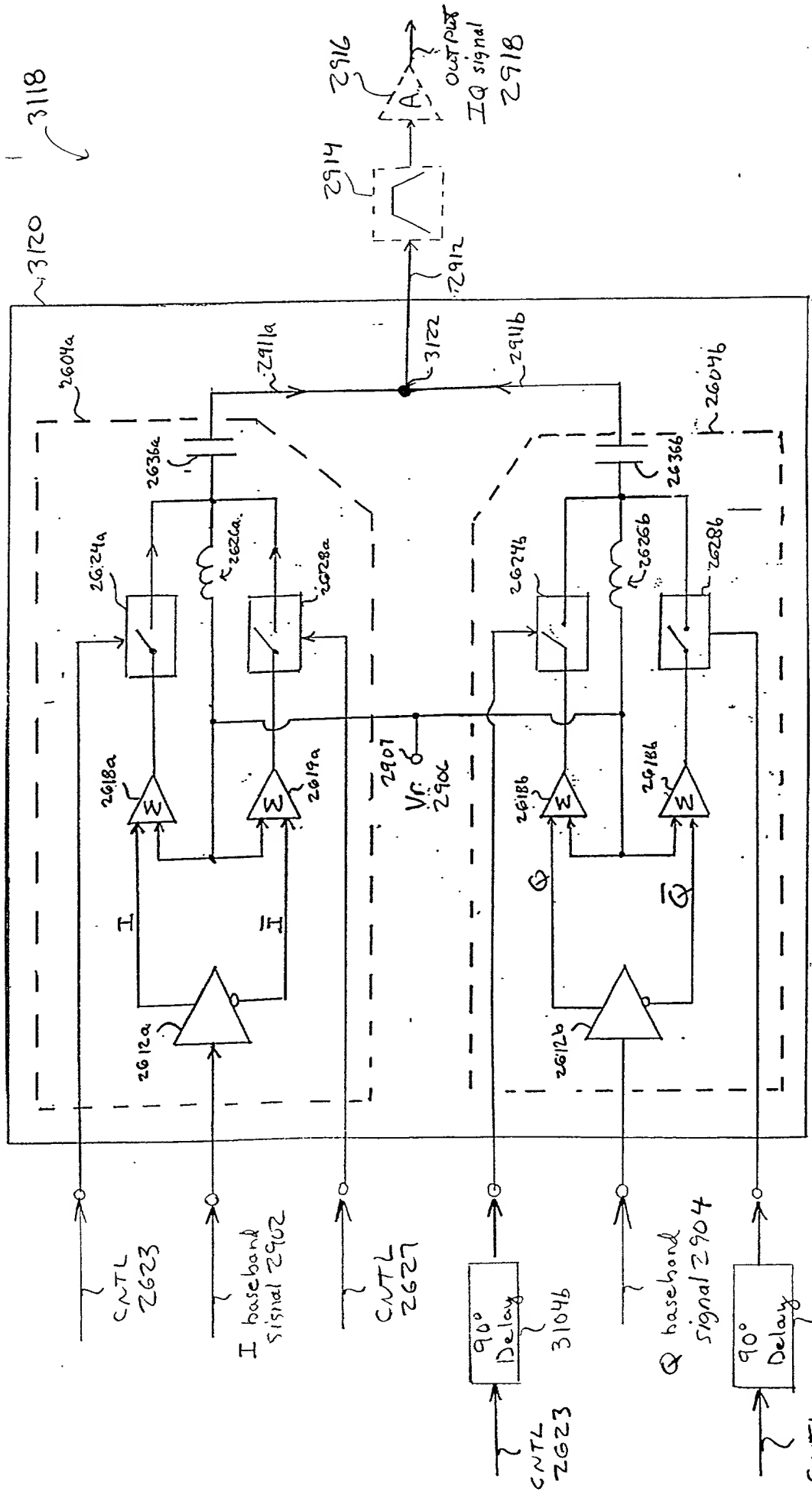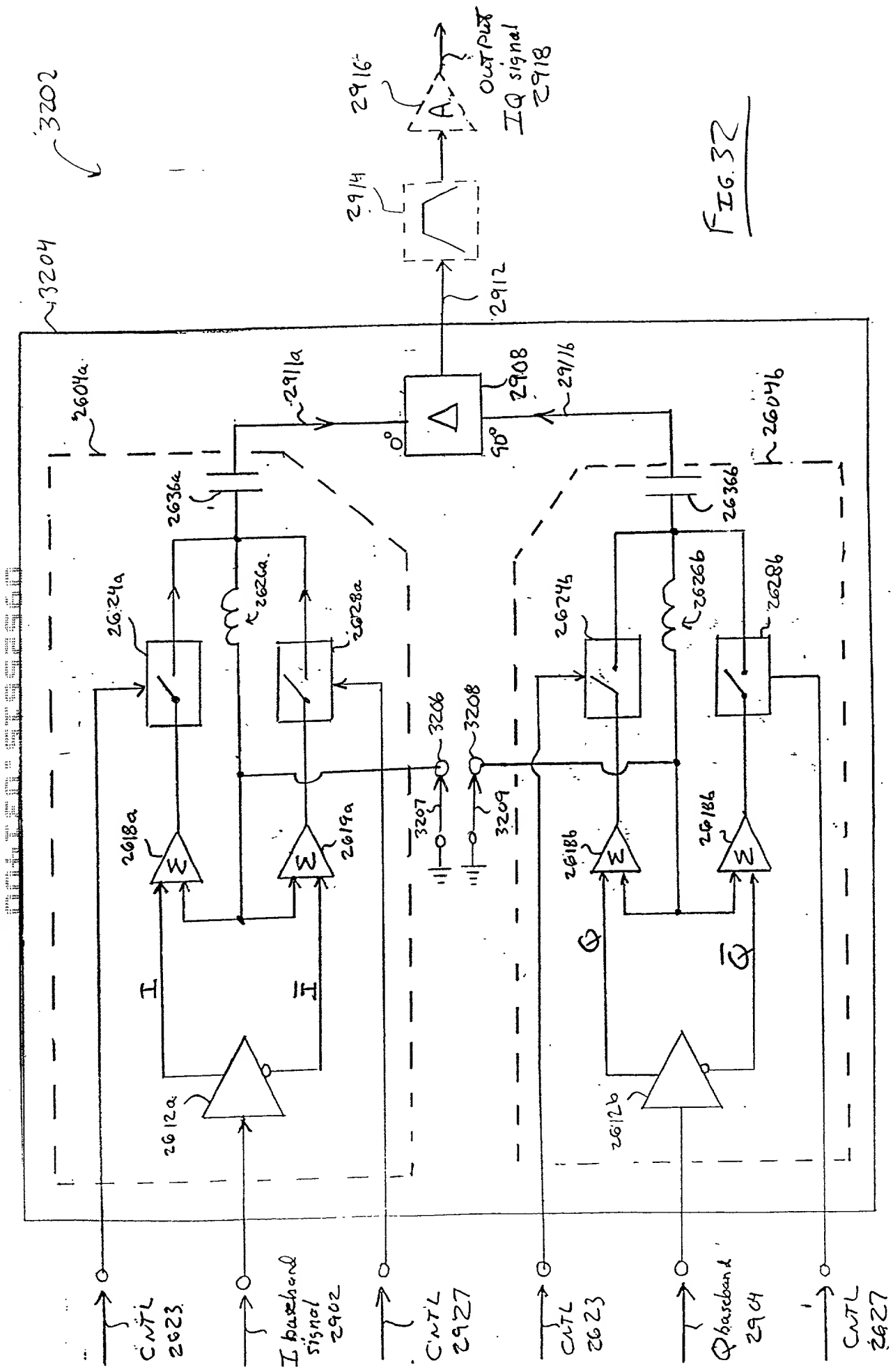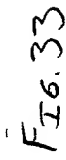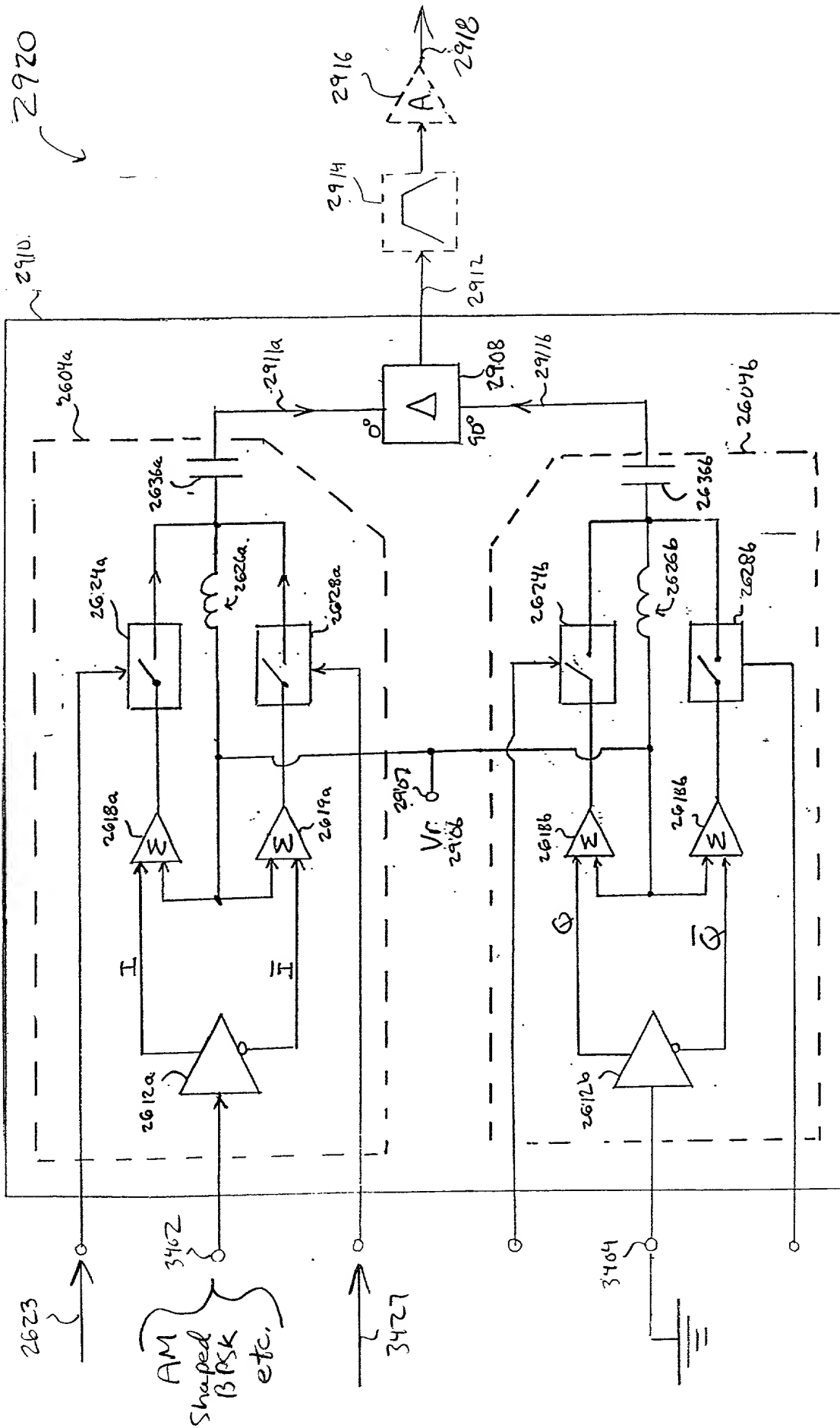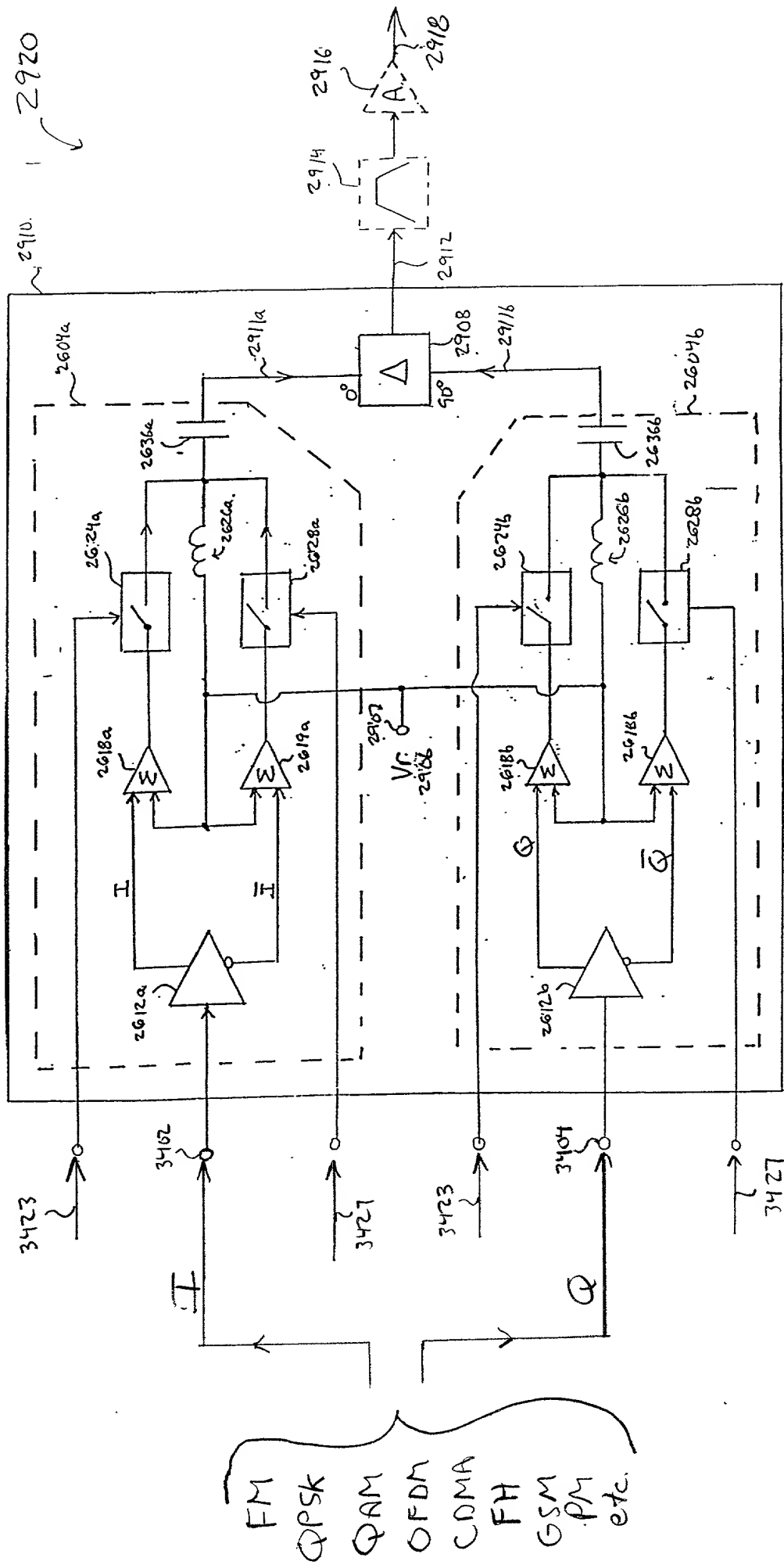
FM
QPSK
QAM
OFDM
CDMA
FH
GSM
PM
etc.

FIG. 35A: Base Station IS-95 Requirements

FIG. 35B: Mobile IS-95 Requirements

FIG. 36: Conventional Transmitter

3600

Input signal 3602
BB Processor 3604
I signal 3606a
Q signal 3606b
BB Filter 3608
3610
X 3612
LO₁ 13
3614
A 3616
3618
SAW 3620
3622
X 3624
LO₂ 3625
3626
PA 3628
3630
3632
3634
3636

FIG. 37A: CDMA Transmitter

3706a

I

3714a

3715a

3714b

FIG. 37B

3706b

Q

3714c

3715b

3714d

FIG 37C

FIG. 370

3708

3716n

3718

3716b

3762

3716a

n/T_s

$2/T_s$

$1/T_s$

Freq

FIG. 37E

Fig. 37F CDMA Transmitter

FIG. 38: CDMA CMOS CHIP

3900

837 MHz

3905

Attn & CABLE 3906

HP 4106A test set

3904

Voc   Vcc

3903

Modulator 2910

VR

I   3902a   8 dB Attn

Q   3902b   8 dB Attn

2627   Control Signal Generator 2644

2623

2645   279 MHz -14 dBm

HP E4433B Generator

I   Q

Fig. 39.

Base Station

4002

FIG. 40

RHO	0.9970
EVM	5.51%
PHASE ERROR	1.80°
MAGNITUDE ERROR	4.53%
CARRIER INSERTION	-37.91 dB
PA POWER OUT	28.06 dBm

FREQUENCY (MHz) (Mobile Station)

4102

	LOW	MIDDLE	HIGH
RHO	0.9892	0.9969	0.9892
EVM	10.39%	5.54%	10.39%
PHASE ERROR	4.47°	2.24°	4.08°
MAGNITUDE ERROR	6.84%	4.21%	8.27%
CARRIER INSERTION	-40.15 dB	-44.58 dB	-35.27 dB
PA POWER OUT	27.36 dBm	28.11 dBm	27.55 dBm

FIG. 41
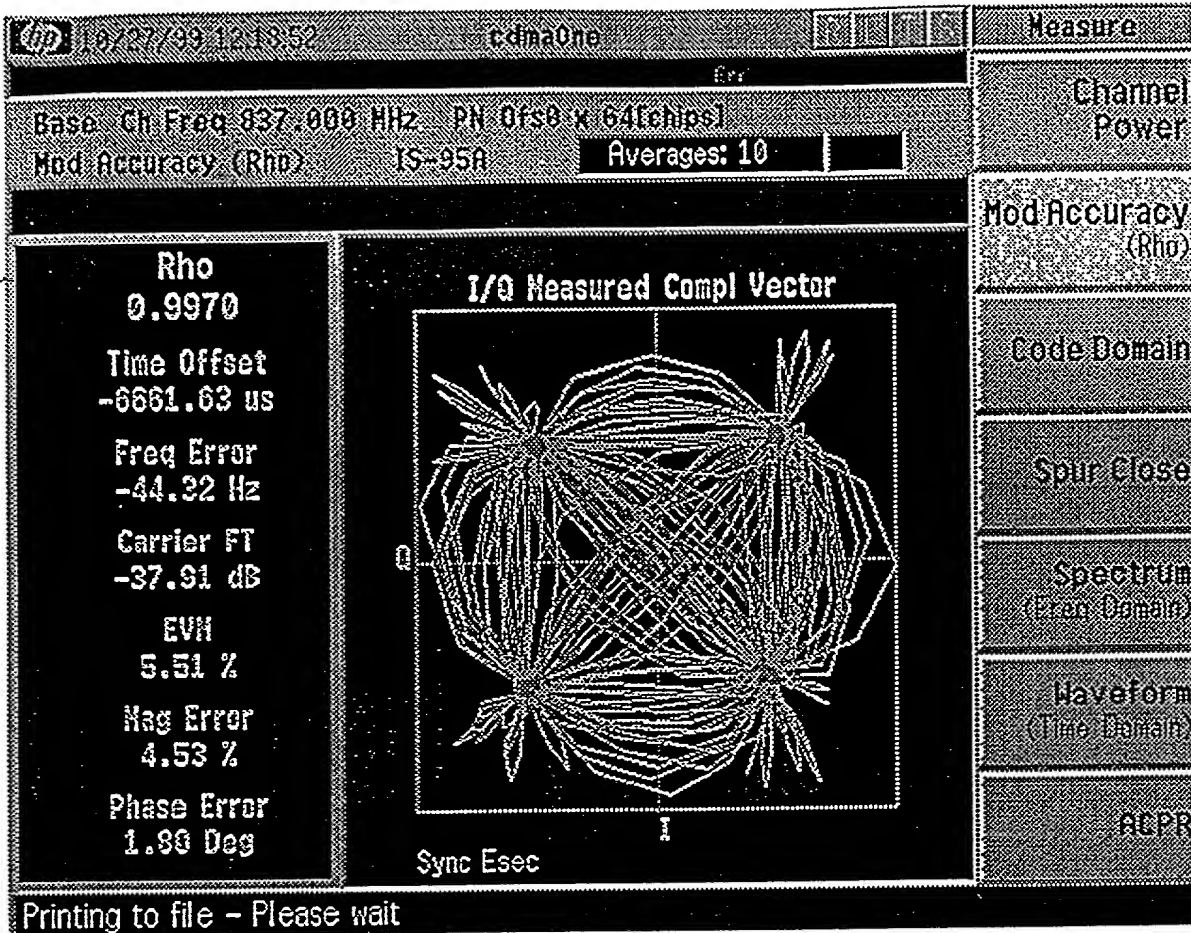
Base Station Constellation for Pilot Channel Test

FIG. 42

4302
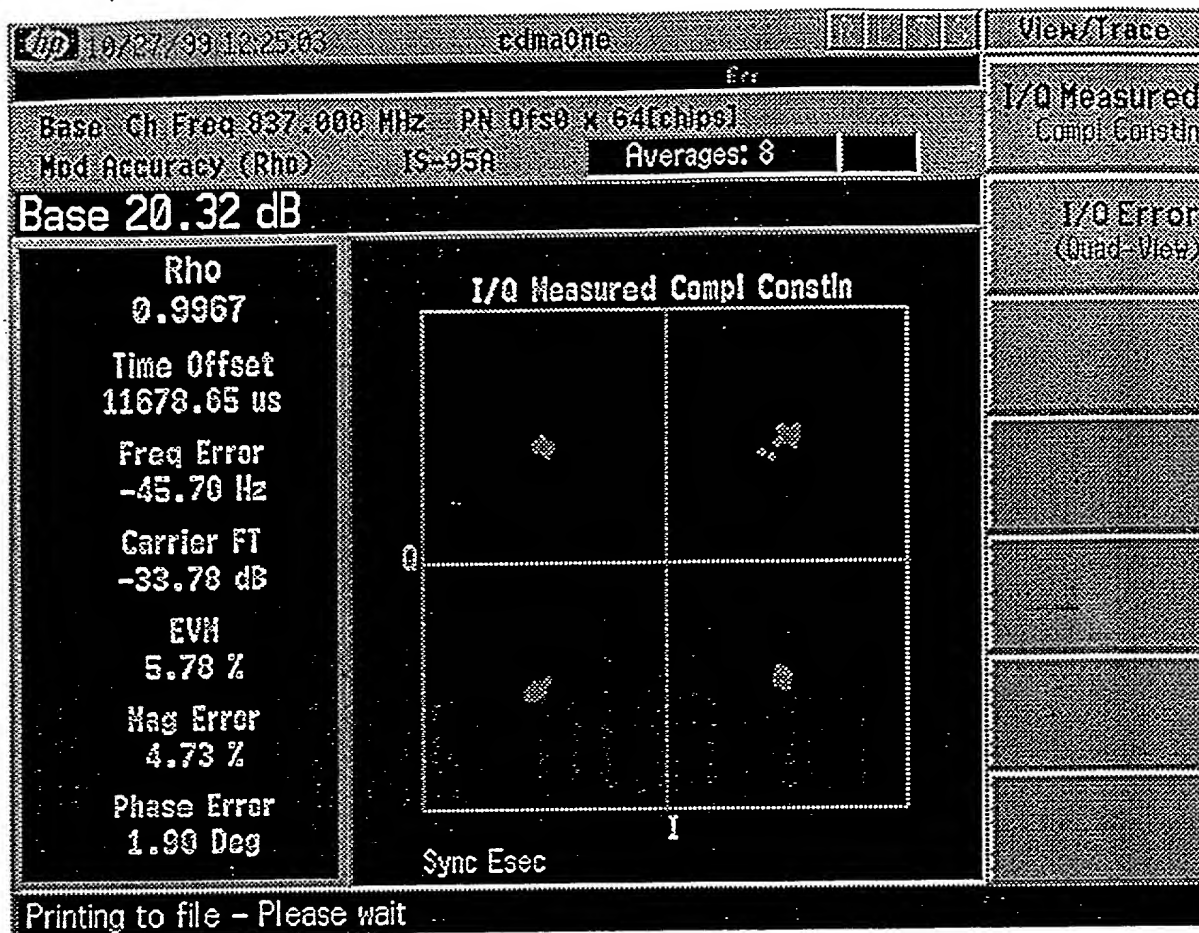
Base Station Sampled Constellation

FIG. 43

4402
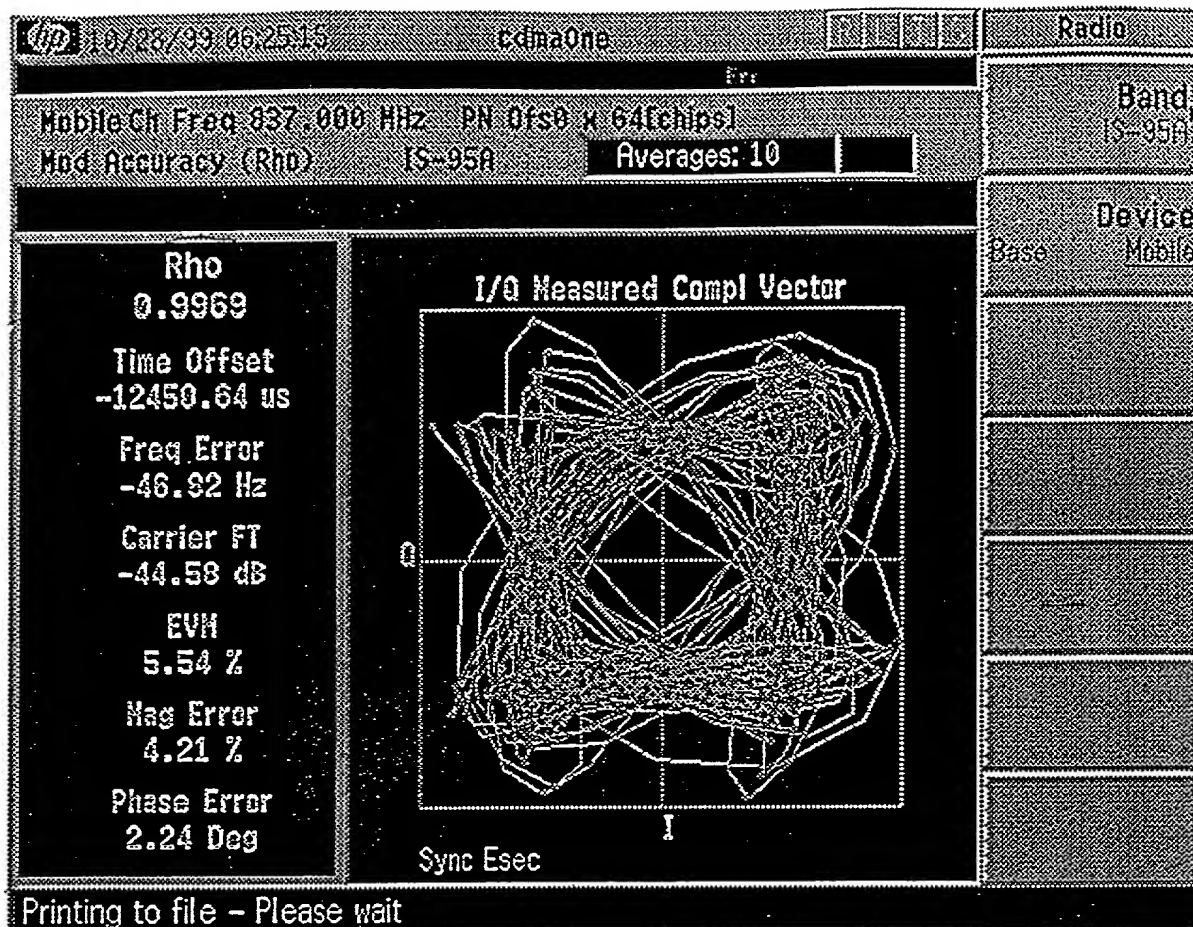
Mobile Station Constellation for Access Channel Test

FIG. 44

4502
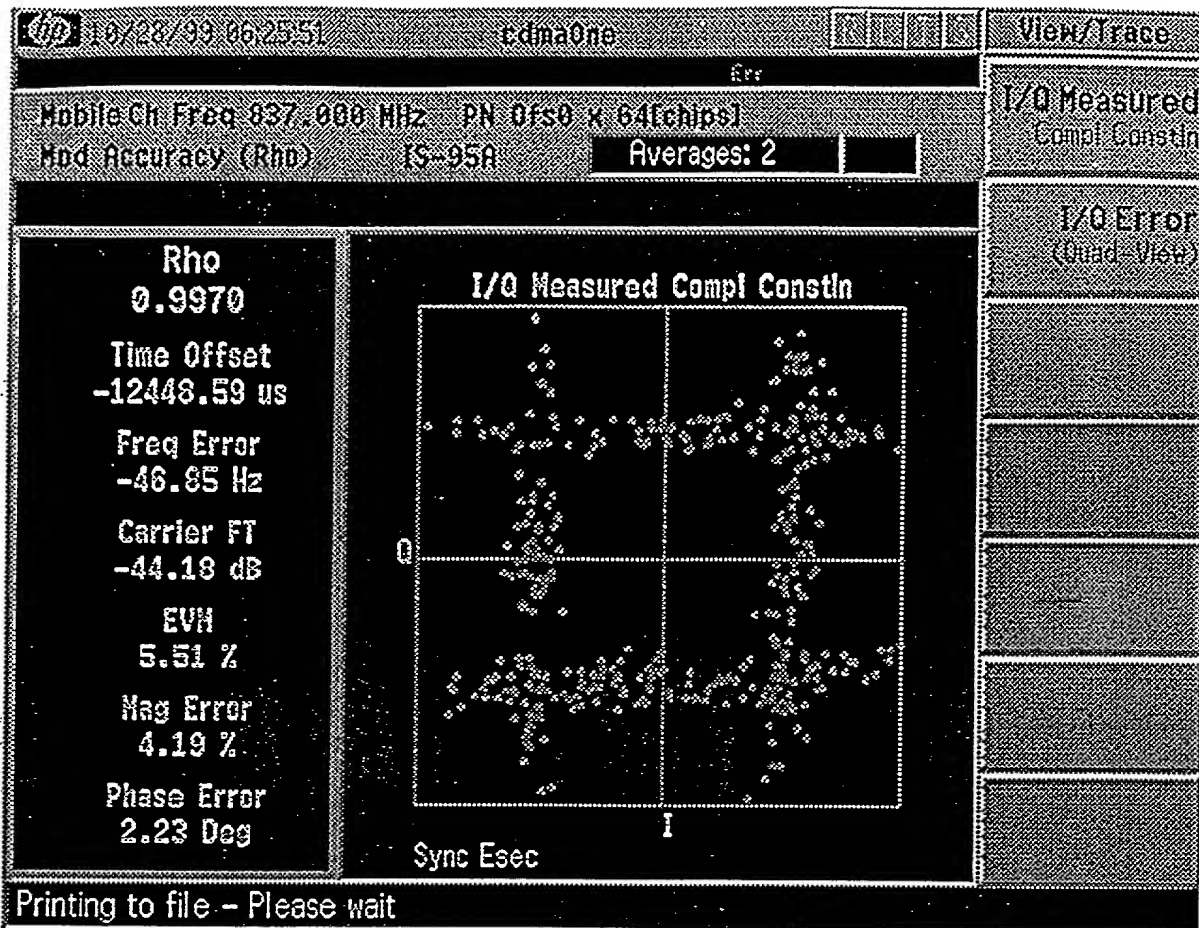
Mobile Station Sampled Constellation

FIG. 45
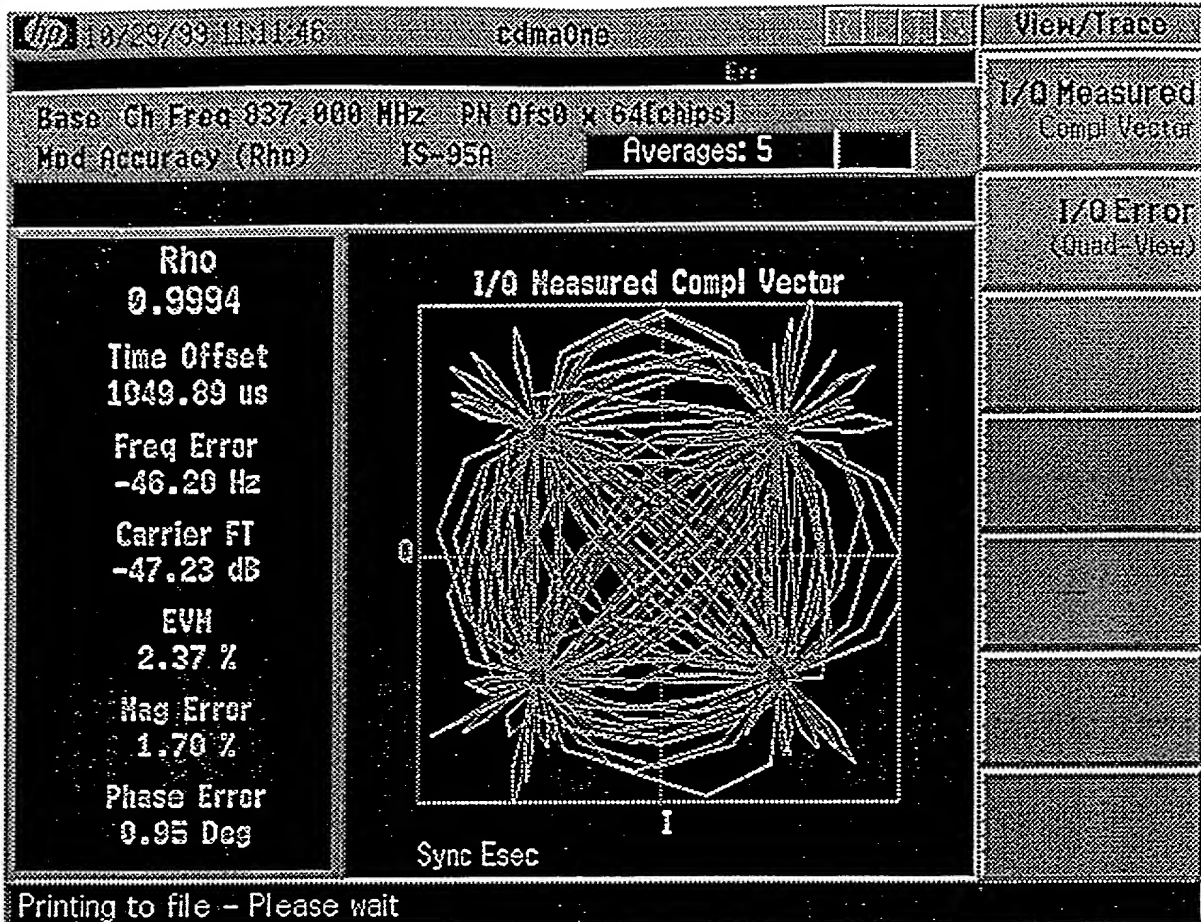
Base Station Constellation using only H/P Test Equipment

FIG. 46

4702
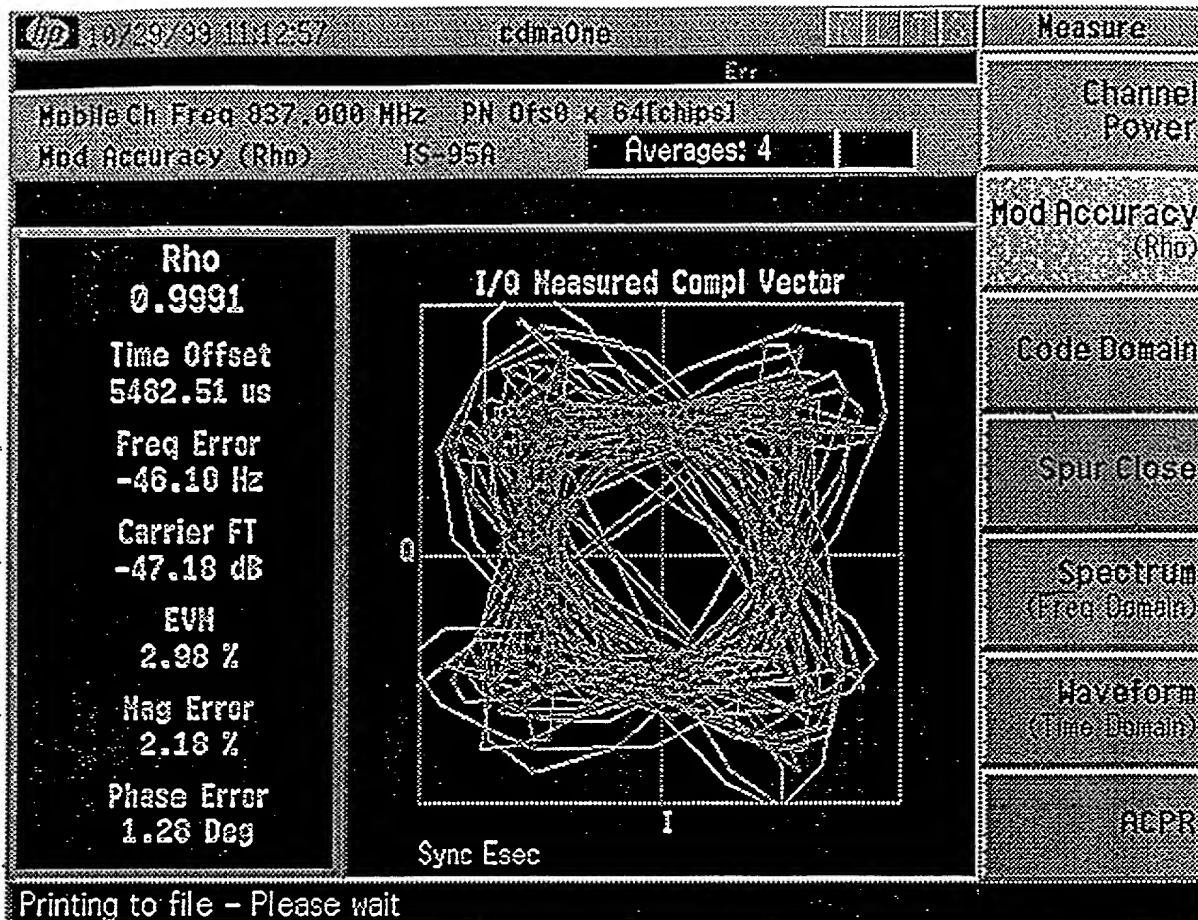
Mobile Constellation using only H/P Test Equipment

FIG. 47

4862

FIG. 48

4902
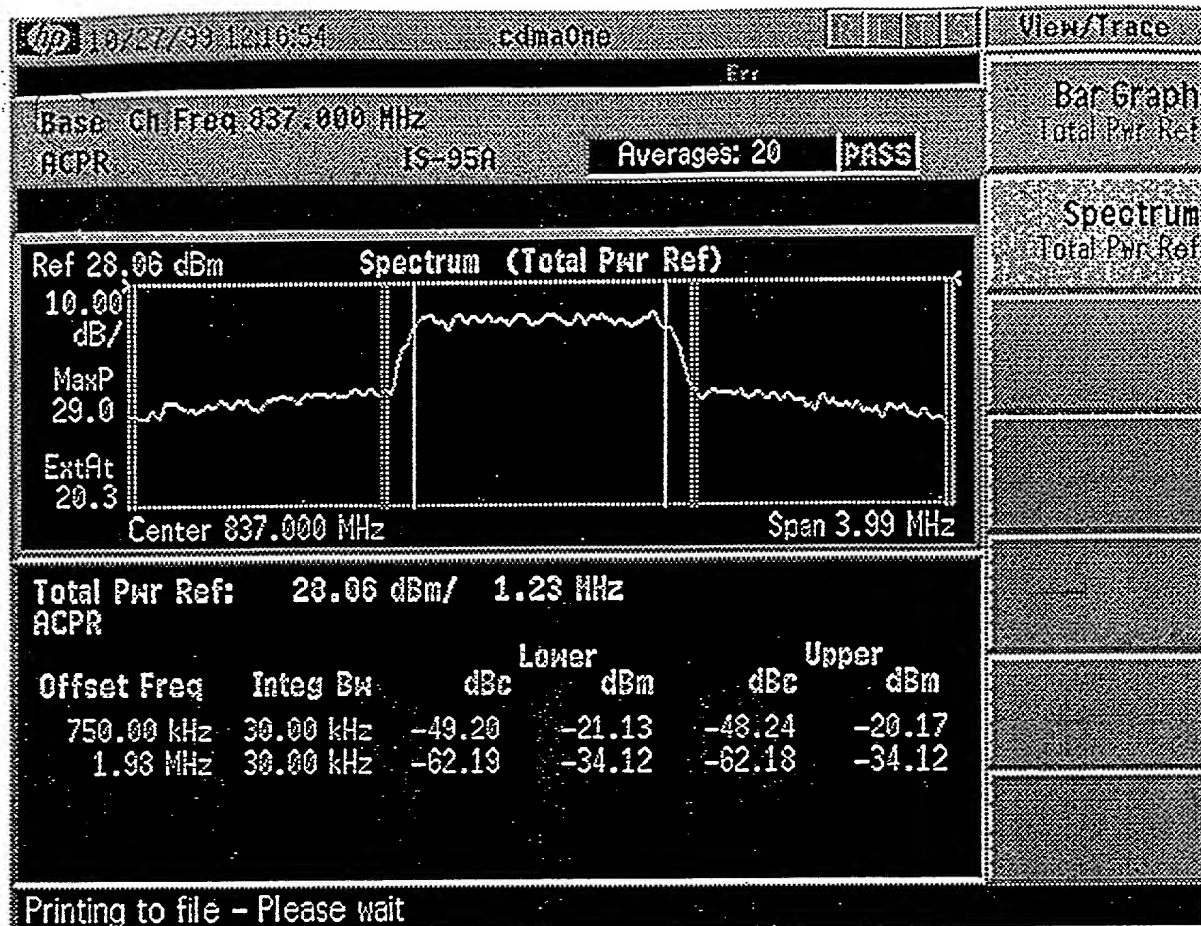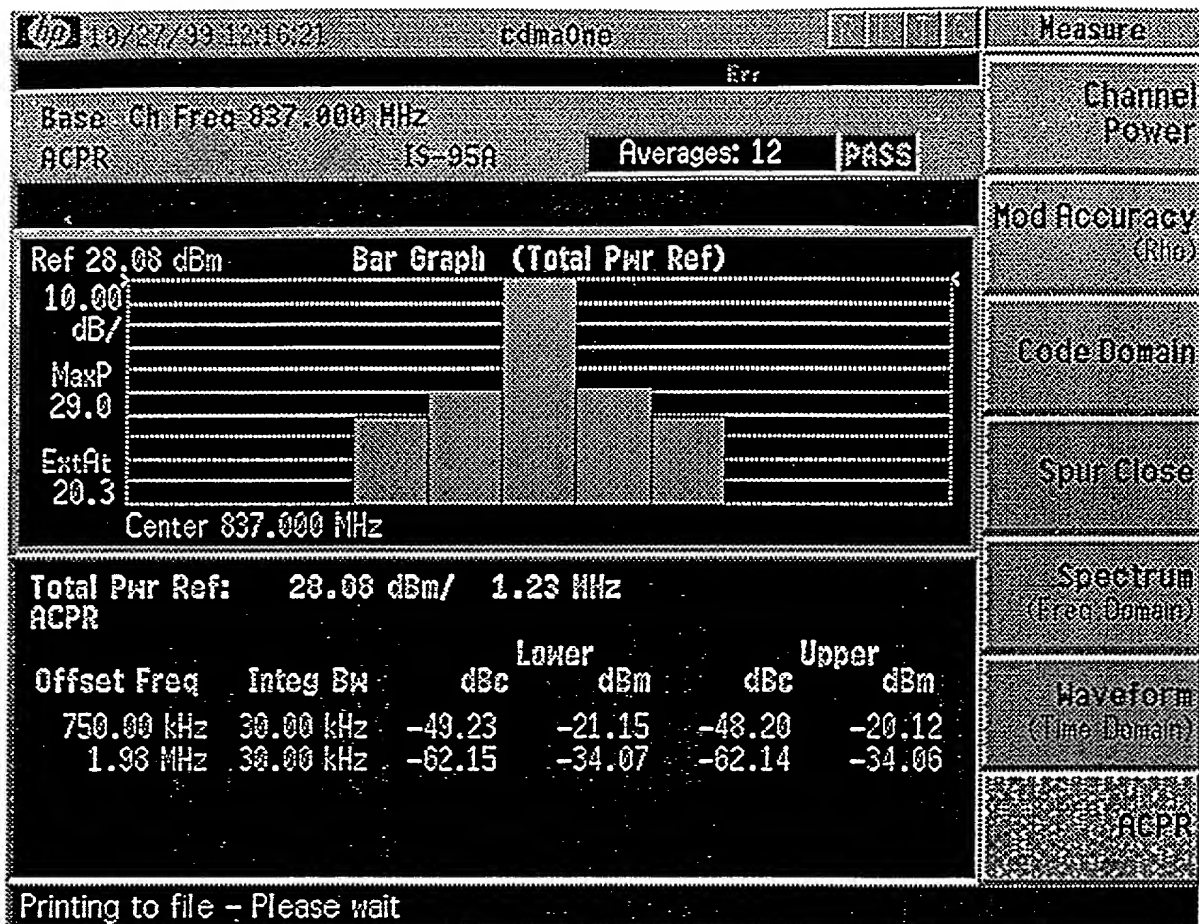
Base Station Spectral Response with Mask

FIG. 49
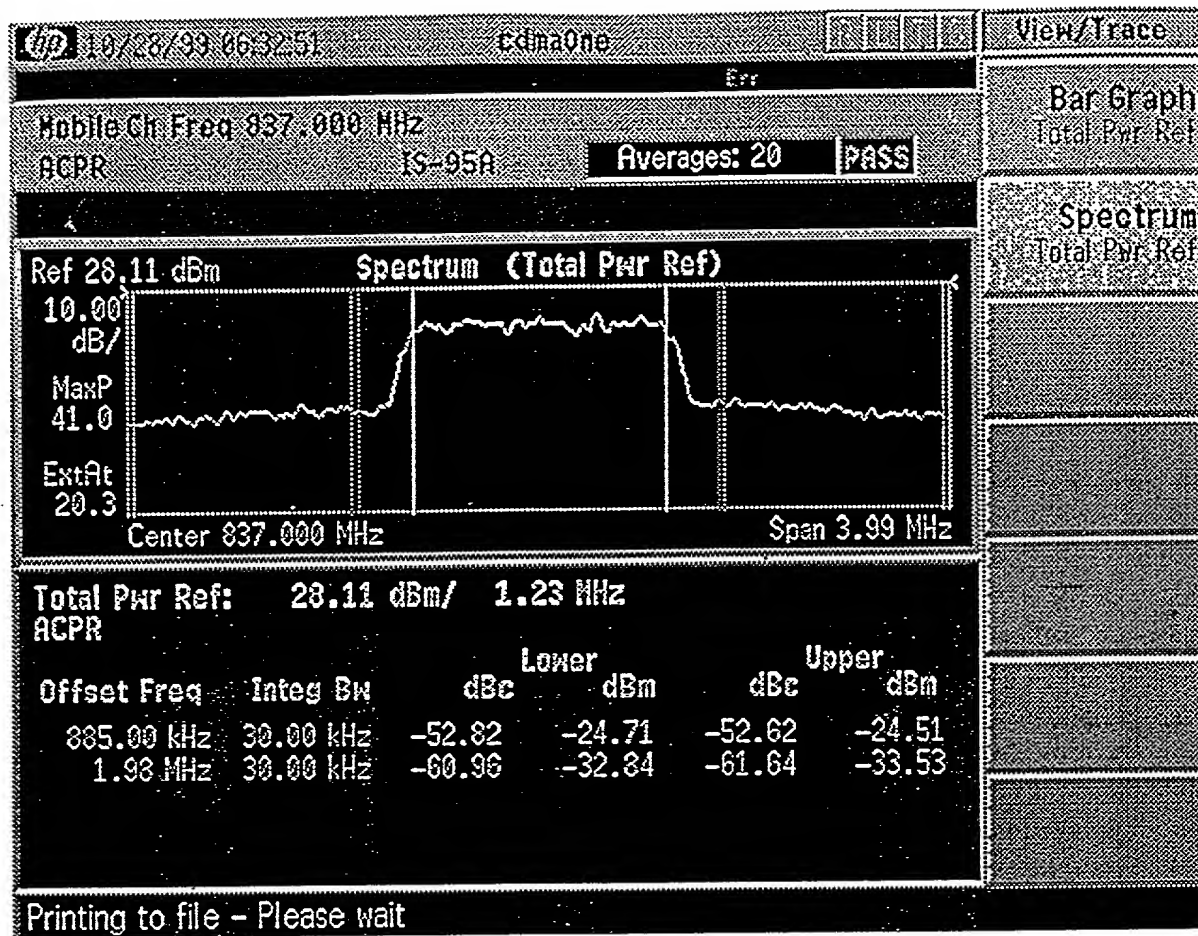
FIG. 50
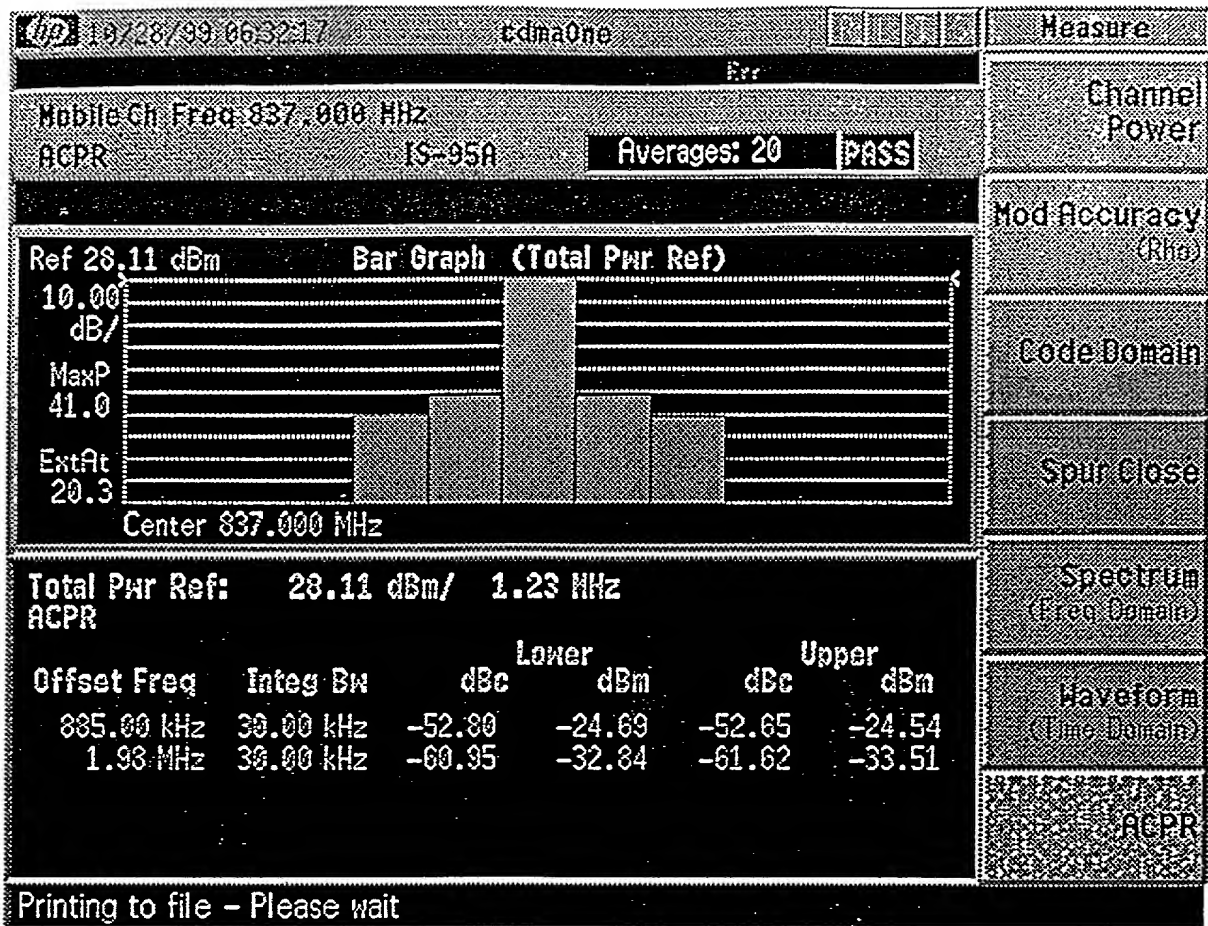
Figure 3.2-2 Mobile Station Spectral Response with Mask

FIG. 51

5202
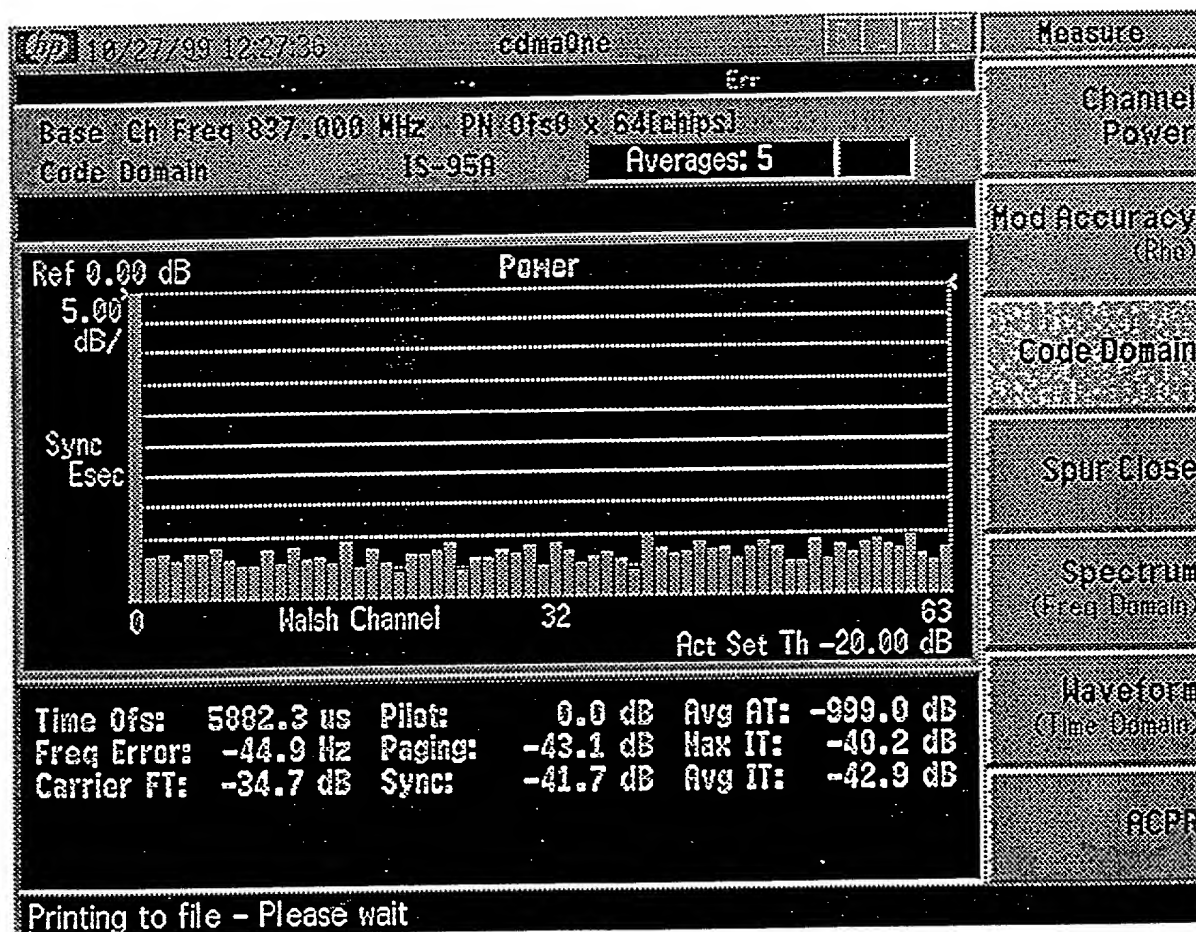
CDMA Crosstalk

FIG. 52A

Sequence for IQ Input Level Variance

CDMA IS-95A
Rho vs Shaped IQ input Level

FIG 52B

CDMA IS-95A
Transmitted Channel Power vs Shaped IQ Input Level

FIG 52C

FIG 52D

CDMA IS-95A
ACPR vs Shaped IQ Input Level

FIG. 52E

CDMA IS-95A
EVM and Magnitude Error vs
Shaped IQ Input Level

CDMA IS-95A
Carrier FT vs Shaped IQ Input Level

Sequence for LO Variance

CDMA IS-95A
Rho vs LO Level

FIG. 52H

CDMA IS-95A
Transmitted Channel Power vs LO Level

FIG. 52I

CDMA IS-95A
ACPR vs LO Level

FIG. 52J

CDMA IS-95A
EVM and Magnitude Error vs
LO Level

FIG. 52k

CDMA IS-95A
Carrier FT vs LO Level

i

CDMA IS-95A
Carrier FT vs Shaped IQ Input Level

FIG. 52L

CDMA IS-95A
ACPR vs Shaped IQ Input Level

FIG. 52M

FIG.52N

CDMA IS-95A
Rho vs Shaped IQ input Level

FIG 52O

CDMA IS-95A
EVM, Magnitude Error and Phase Error
vs Shaped IQ Input Level

Sequence for IQ Input Level Variance

FIG. 52P

CDMA IS-95A Mobile Transmitter@+3.3V
Rho vs Shaped IQ input Level

FIG. 52Q

CDMA IS-95A Mobile Transmitter@+3.3V
Transmitted Channel Power vs Shaped IQ Input Level

FIG. 52R

CDMA IS-95A Mobile Transmitter@+3.3V
ACPR vs Shaped IQ Input Level

FIG. 52S

CDMA IS-95A Mobile Transmitter@+3.3V
EVM, Magnitude Error and Phase Error
vs Shaped IQ Input Level
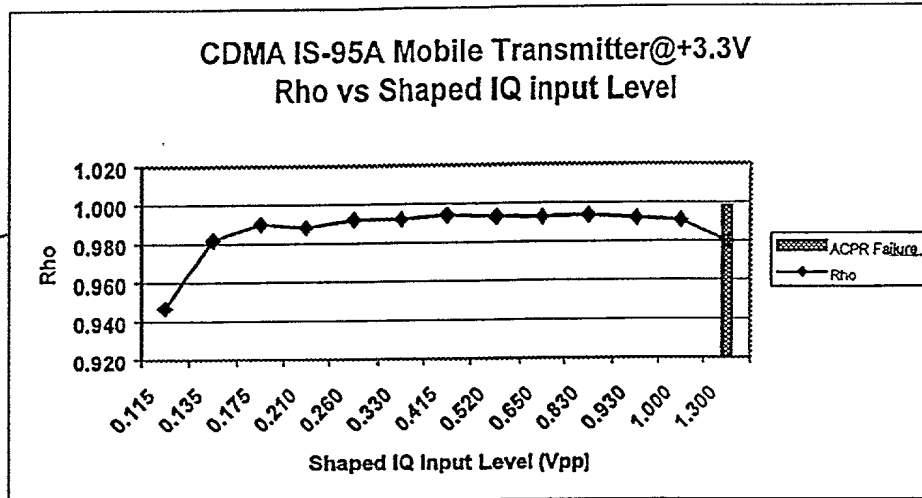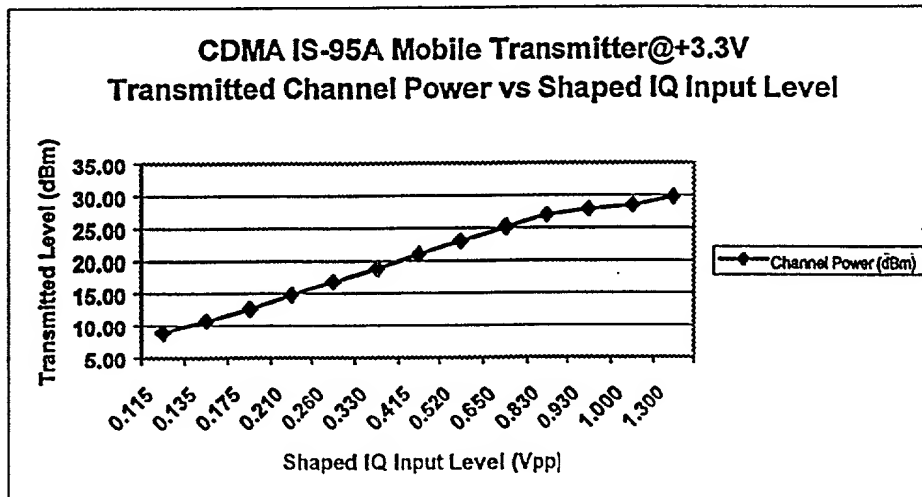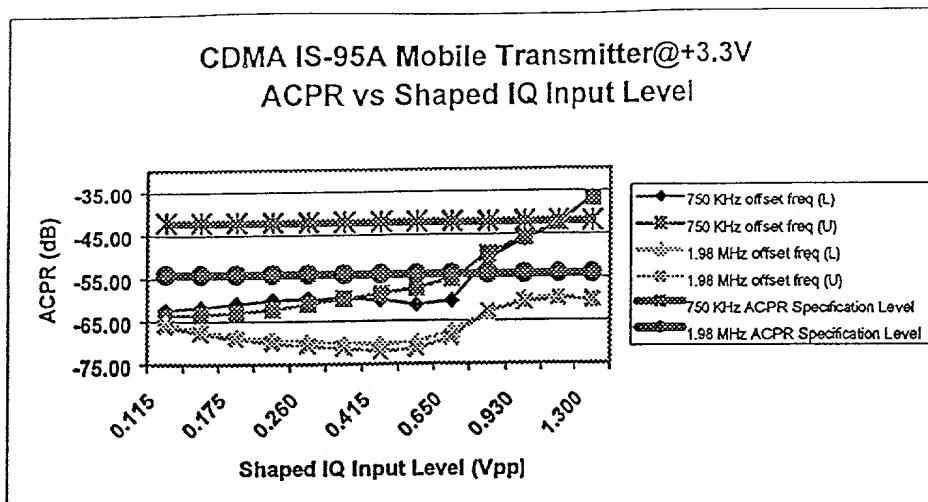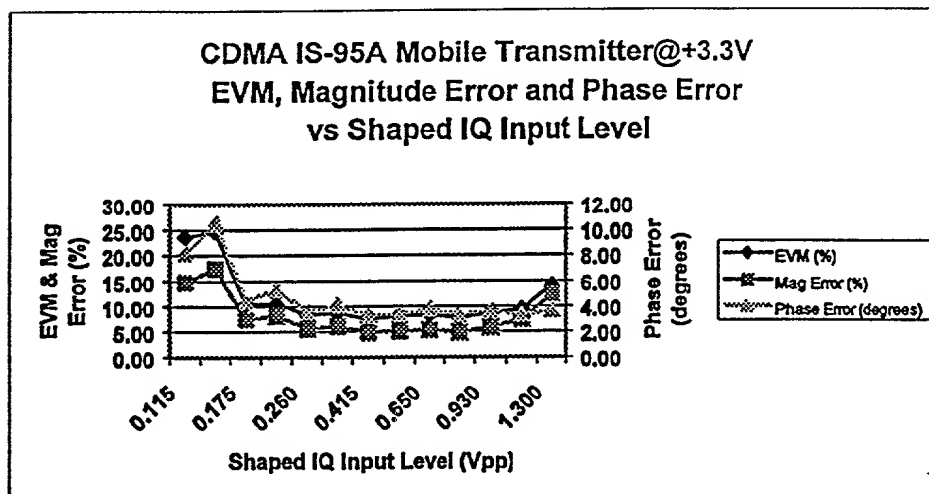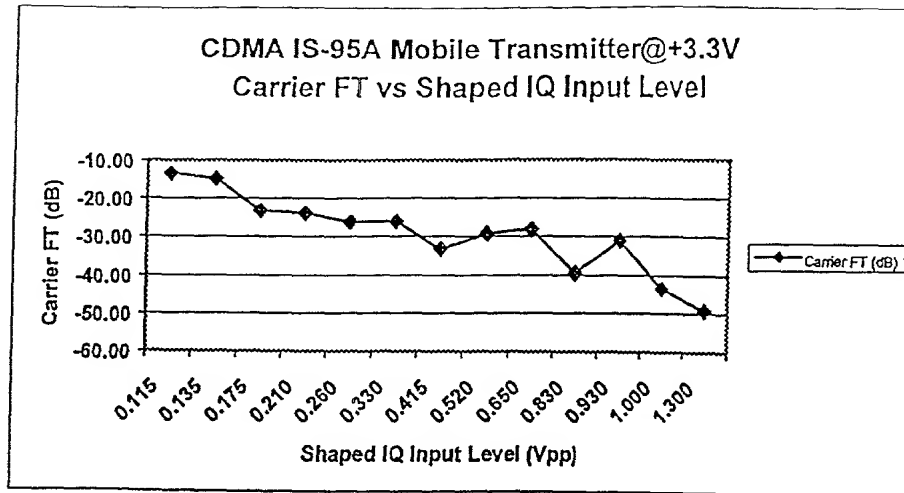
FIG. 52T

Figure 3.6-5

Sequence for LO Variance

FIG. 52U

Figure 3.6-6

CDMA IS-95A Mobile Transmitter@+3.3V
Transmitted Channel Power vs LO Level

Transmitted Level (dBm)

30
29
28
27
26
25

-16 -14 -12 -10 -8 -6

LO (dBm)

Channel Power (dBm)

FIG. 52U

CDMA IS-95A Mobile Transmitter@+3.3V
ACPR vs LO Level

ACPR (dB)

-40
-45
-50
-55
-60
-65

-16 -14 -12 -10 -8 -6

LO (dBm)

750 KHz offset freq (L)
750 KHz offset freq (U)
1.96 MHz offset freq (L)
1.96 MHz offset freq (U)
750 KHz ACPR Specification Level
1.96 MHz ACPR Specification Level

FIG. 52W

FIG. 52X

CDMA IS-95A Mobile Transmitter@+3.3V
EVM and Magnitude Error vs
LO Level

FIG. 52Y

CDMA IS-95A Mobile Transmitter@+3.3V
Carrier FT vs LO Level

Quantity	Description	Voltage	Total Current	Power
2	· Cores	3.3	4mA	13.2mW
2	Baseband Interface Circuits with/BW Limit	3.3	6mA	21.8mW
1	Clock Circuit	3.3	5mA	20.0mW
			Sub Total	54.0mW

FIG. 52Z

Fig. 53A

Amplitude

PN code
5316

5306

t_0

Time

FIG. 53B

$S320a$ $S320b$ $S320c$ $S320n$
$S312$

$1/T_s$ $2/T_s$ n/T_s

Freq

FIG. 53c

FIG. 54A

PN
code
5422

5420

t_1

t_1

t_0

t_6

FIG. 54B

I

5402a

5406a

LPF

5407a

5466a

Modulator
2604a

5409a

0°

5410

5408a

5413

5412

5424

IQ-
output
5428

90°

5420

5430

5406b

Q

5402b

LPF

5406b

5457b

Modulator
2604b

5411

90°

5413

5415

2642

Control
Signal
Generator

5416

5418

Clk
Driver

5421

5422

Code
Generator

5423

FIG. 54C

FIG. 55A

FIG. 5.5B

FIG. 55C

FIG. 550

5600

5601

2608

A

Output Signal 5636

2606

5634

5632

5628

Cblk

5614

5616

5618

5620

5622

5624

5626

5630

Cblk

R or L

5610

5606

I

5604

5608

II

5612

R or L

CNTL 2623

5602

CNTL 2621

CNTL Signal generator

2642

Fig. 56A

Amplitude

5602

5650a

"1/Ts

5650b

2/Ts

5650c

3/Ts

5650n

n/Ts

Frequency

5614

FIG. 56B

Amplitude

S652a

S652b

S652c

S656

S652n

1/Ts   2/Ts   3/Ts   n/Ts   Frequency

S632

FIG. 56c

5600

5601

Output Signal 5636

2608

A

2606

5634

5632

5628

C_BLK

5614

5618

5616

S636

S D

5620

5624

5622

5630

C_BLK

5626

D S

5638

5614

R_ar_L

5610

I

5606

5604

5612

R_or_L

II

5608

CNTL 2623

5602

CNTL 2627

CNTL Signal Generator

2642

FIG. 56D

FIG 57

Fig. 58A

Fig. 58B

Fig. 58C

FIG. 59

5900

5902

Output signal 5716

5714 A

5712
5711

5906 0°
0°

S601a
S601b

5706
5708

I baseband 5702
Q Baseband 5704

CNTL 2643
CNTL 2627
CNTL 2623
CNTL 2627

90° Delay 5904a
90° Delay 5904b

S604a
S604b

S610a'
S610b'
S612a
S612b

RorL
RorL
RorL
RorL

S616a
S616b
S620a
S620b
S622a
S622b

S628a
S628b
S630a
S630b

S632
S632

Calk
Calk
Calk
Calk

6000

6002

6001a

CNTL 2643

I baseband 5702

CNTL 2627

S604a

S610a'

S616a

S628a

Cblk

SG20a

SG22a

SG30a

Cblk

S612a

S632

S706

S601b

S904a

90° Delay

CNTL 2623

Q Baseband 5704

CNTL 2627

S904b

90° Delay

S604b

S610b

S616b

S628b

Cblk

SG20b

SG22b

SG30b

Cblk

S612b

S632

S708

6004

S711

S712

S714

A

Output signal 5716

FIG. 60

FIG.61

6200

6202

Receive an input baseband signal

6204

Differentially sample the baseband signal according according to a first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image

6206

Minimize DC offset voltages between sampling modules during the differential sampling in step 6204

6208

Select a desired harmonic (or subset of harmonics) of interest for transmission

6210

Amplify the selected harmonic(s)

6212

Transmit the selected harmonic(s) over a communications medium

FIG.62

6300

6202

Receive an input baseband signal

Convert the (single-ended) input baseband signal into a differential signal
having first and second signal components, where the second component
is an inverted version of the first component
~ 6302

Add a DC reference voltage to both of the differential signal components,
resulting in a first combined signal and second combined signal
~ 6304

Generate a first control signal and a second control signal
that have a common frequency but are phase-shifted with respect to each other,
and that have pulse widths (or apertures) of T_A that are established to improve
energy transfer to a desired harmonic of the control signal frequency
~ 6306

6204,
6206

Sample the first combined signal according to the first control signal
to generate a first harmonically rich signal
~ 6308

Sample the second combined signal according to the second control signal
to generate a second harmonically rich signal
~ 6310

Combine the first harmonically rich signal and the second harmonically
rich signal to generate a third harmonically rich signal that has minimal
carrier insertion in the harmonic images
~ 6312

Select a desired harmonic (or subset of harmonics) for transmission
~ 6208

FIG. 63

6400

Receive an input baseband signal ⟋6202

Convert the (single-ended) input baseband signal into a differential signal ⟋6402
having first and second signal components, where the second component
is an inverted version of the first component

Generate a first control signal and a second control signal ⟋6404
that have a common frequency but are phase-shifted with respect to each other,
and that have pulse widths (or apertures) of T_A that are established to improve
energy transfer to a desired harmonic of the control signal frequency

Shunt the first differential signal component to ground according to the ⟋6406
first control signal to generate a first harmonically rich signal

Shunt the second differential signal component to ground according to the ⟋6408
second control signal to generate a second harmonically rich signal

Combine the first harmonically rich signal and the second harmonically ⟋6410
rich signal to generate a third harmonically rich signal that has minimal
carrier insertion in the harmonic images

6204,
6206

Select a desired harmonic (or subset of harmonics) for transmission ⟋6208

FIG. 64

6500

Receive an I baseband signal and a Q baseband signal ~6502

Differentially sample the I baseband signal according to a first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting I harmonically rich signal ~6504

Differentially sample the Q baseband signal according to a first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting Q harmonically rich signal ~6506

Minimize DC offset voltages between sampling modules during the differential sampling steps ~6508

Combine the I harmonically rich signal and the Q harmonically rich signal to generate an IQ harmonically rich signal ~6510

Select a desired harmonic (or subset of harmonics) of interest for transmission ~6512

Amplify the selected harmonic(s) ~6514

Transmit the selected harmonic(s) over a communications medium ~6516

FIG.65

6600

Receive an I baseband signal and a Q baseband signal — 6602

Differentially shunt the I baseband signal to ground according to first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting I harmonically rich signal — 6604

Differentially shunt the Q baseband signal to ground according to first and second control signals that have pulse widths (or apertures) established to improve energy transfer to a desired harmonic image in the resulting Q harmonically rich signal — 6606

Combine the I harmonically rich signal and the Q harmonically rich signal to generate an IQ harmonically rich signal — 6608

Select a desired harmonic (or subset of harmonics) of interest for transmission — 6610

Amplify the selected harmonic(s) — 6612

Transmit the selected harmonic(s) over a communications medium — 6614

FIG. 66

6700

Receive an input baseband signal ~ 6701

Generate a sub-harmonic clock signal ~ 6702

Generate spreading code, and send to clock modulator and amplitude shaper ~ 6704

Modulate the sub-harmonic clock signal with the spreading code ~ 6706

Generate a first control signal and a second control signal based on the spread/modulated clock signal, the first and second control signals having pulse widths (or apertures) of T_A that are established to improve energy transfer to a desired harmonic of the control signal frequency ~ 6708

Smooth and shape the amplitude of the input baseband signal so that it corresponds with the spreading code (i.e. synchronize zero crossings in-time) ~ 6710

Filter the shaped input signal to remove high frequency components ~ 6712

Sample the shaped and filtered signal in a balanced and differential manner according to the first and second control signals ~ 6714

Select a desired harmonic from the harmonically rich signal ~ 6716

Amplify the desired harmonic ~ 6718

FIG. 67

6800

Receive I and Q baseband signals — 6801

Generate a sub-harmonic clock signal — 6802

Generate I and Q spreading codes, and send to clock modulator and amplitude shaper — 6804

Modulate the sub-harmonic clock signal with the I an Q spreading codes to generate I and Q spread clock signals — 6806

Generate a set of I control signals based on the I spread clock signal and a set of Q control signals based on Q spread clock signal, the I and Q control signals having pulse widths (or apertures) of T_A that are established to improve energy transfer to a desired harmonic of the control signal frequency — 6808

Smooth and shape the amplitude of the I and Q input baseband signals to correspond with the respective I and Q spreading codes (i.e. synchronize zero crossings in-time) — 6810

Filter the shaped input signals to remove high frequency components — 6812

FIG. 68A

Sample the shaped/filtered I baseband signal in a balanced and differential manner according to the first and second I control signals ～ 6814

Sample the shaped/filtered Q baseband signal in a balanced and differential manner according to the first and second Q control signals ～ 6816

Combine the I and Q harmonically rich signals ～ 6818

Select a desired harmonic from the harmonically rich signal ～ 6820

Amplify the desired harmonic ～ 6822

FIG. 68B

6900

Receive I baseband signal and a Q baseband signal   — 6901

Generate spreading code, and send to clock modulator and amplitude shaper   — 6902

Generate a clock driver signal that is phase (or frequency) modulated according to the spreading code   — 6904

Generate a clock signal using a VCO that is controlled by the clock driver signal so that the VCO frequency is controlled by the spreading code of the clock driver signal   — 6906

Generate an I control signal and a Q control signal that are based on the spread clock signal, where the I and Q control signals have pulse widths (or apertures) of T_A that are established to improve energy transfer to a desired harmonic of the control signal frequency   — 6908

Filter the I and Q input signals to remove high frequency components   — 6910

Sample the filtered I baseband signal according to the I control signal   — 6912

FIG. 69A

6900
(cont.)

Sample the filtered Q baseband signal according to the Q control signal — 6914

Combine the I and Q harmonically rich signals — 6916

Select a desired harmonic from the harmonically rich signal — 6918

FIG. 69B

FIG 70A

7023

7033

Pulse
Generator → I Control
Signal 7090

7017

7027

÷ 2

7015

Pulse
Generator → Inverted I
Control Signal
7092

7035

7025

Local
Oscillator

7041

7029

7031

7021

7037

180°
Phase
Shifter

÷ 2

Pulse
Generator → Q Control
Signal 7094

7019

7043

7039

Pulse
Generator → Inverted Q
Control Signal
7096

FIG. 70B

Local Oscillator
Signal 7015

Half Frequency LO
Signal 7017

Phase Shifted LO
Signal 7019

Half Frequency
Phase Shifted LO
Signal 7021

I Control Signal
7090

Inverted I Control
Signal 7092

Q Control Signal
7094

Inverted Q Control
Signal 7096

Combined Control
Signal 7045

FIG. 70C

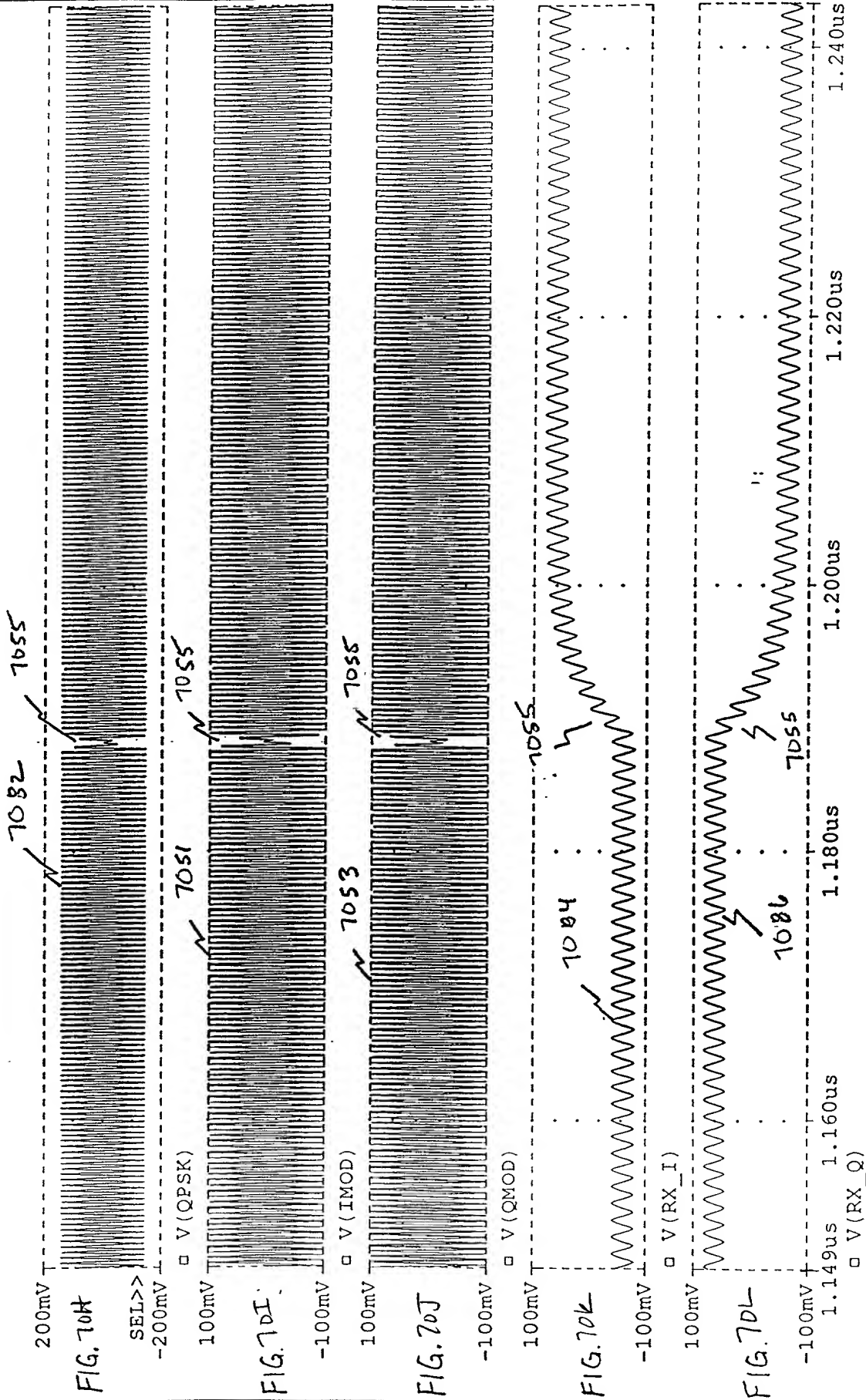(A) IQDEMOD PULSE RELATIONSHIPS TO INPUT RF CARRIER

FIG. 10D

FIG. 70E

21900
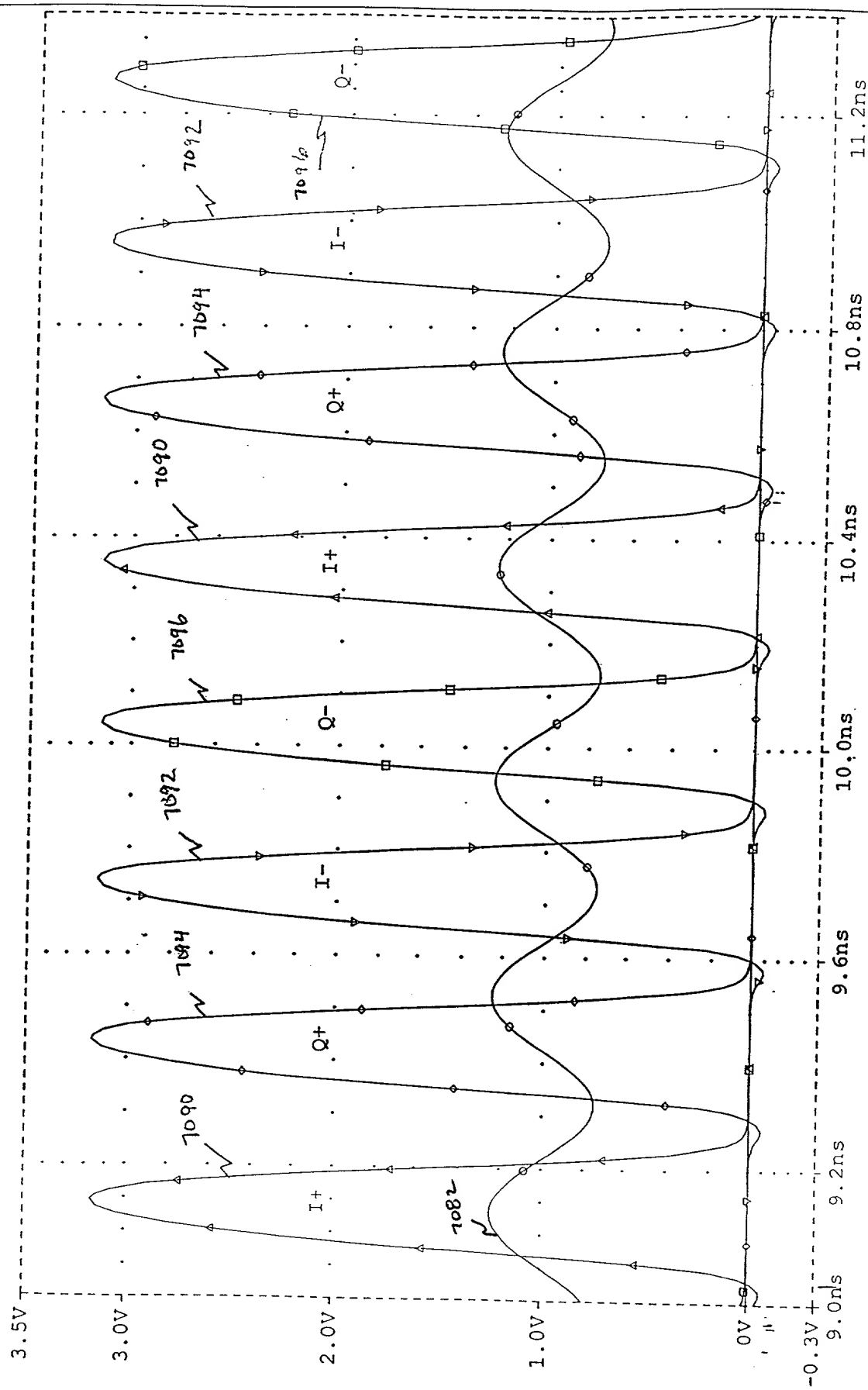
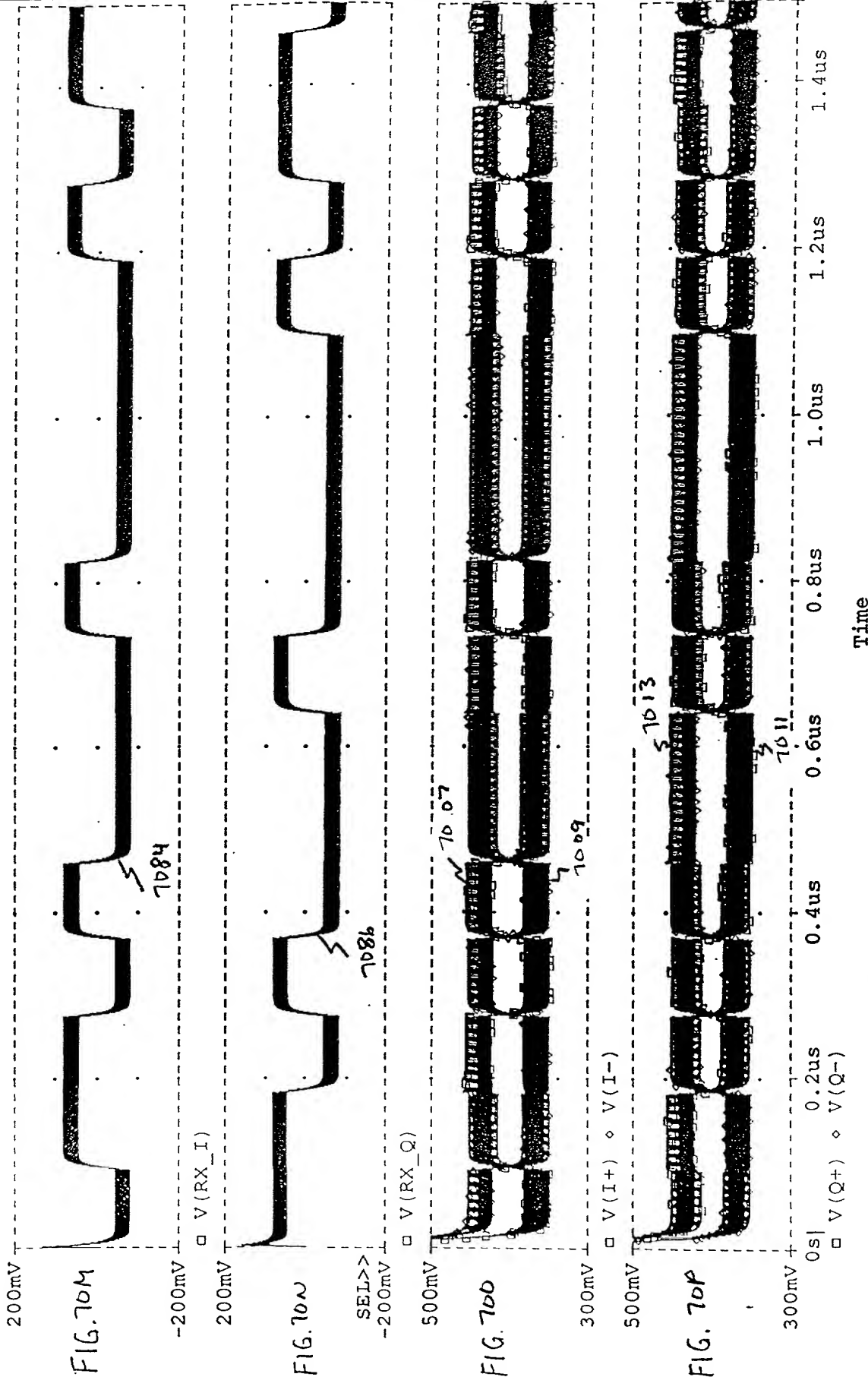(A) IQDEMOD SHOWING TIME RELATIONSHIP OF TX.   I AND Q DATA

FIG.7uF   7647

□ V(TX_I)

FIG.70G   7649

□ V(TX_Q)

1.0V

-1.0V

1.0V

-1.0V

-200mV

0s   0.2us   0.4us   0.6us   0.8us   1.0us   1.2us   1.4us

Time

Page 1
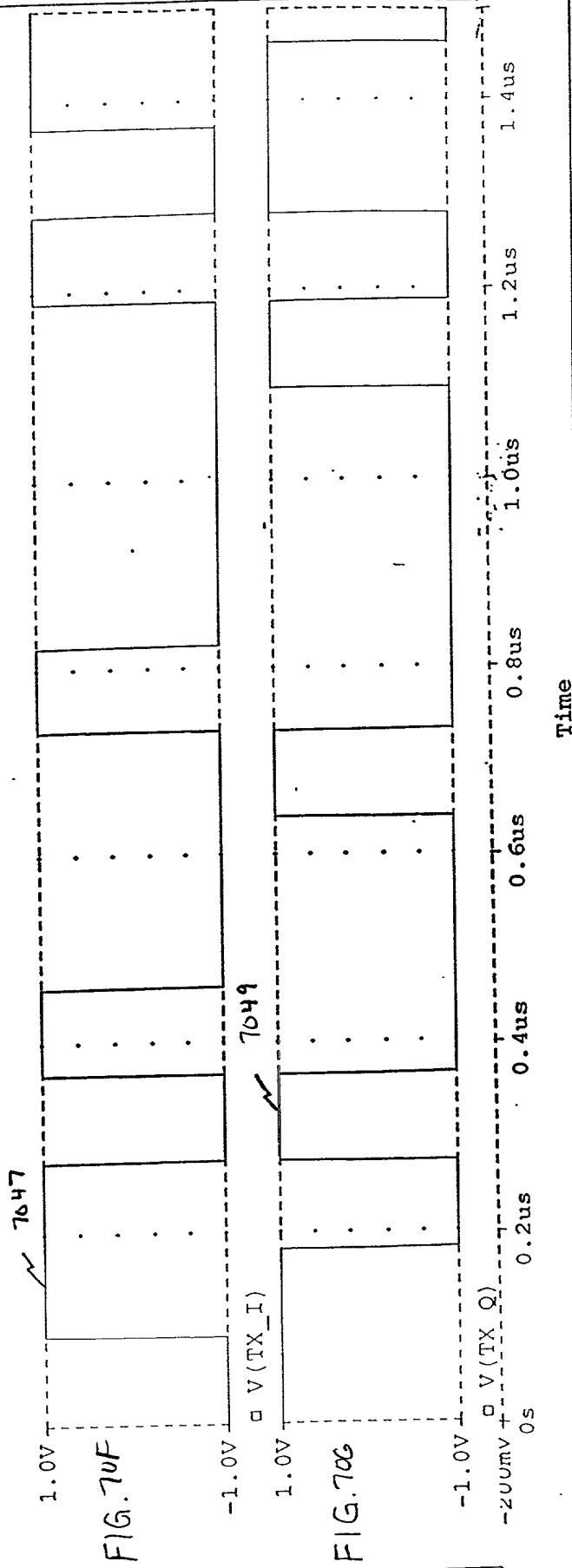
(B) IQDEMOD SHOWING QPSK MOD OUTPUT (TOP) WITH IMOD AND QMOD AND I AND Q DATA (BOTTOM)

FIG. 7oH

200mV
SEL>>
-200mV
□ V(QPSK)

7082 7055
7051

FIG. 7oI

100mV
-100mV
□ V(IMOD)

7055
7053

FIG. 7oJ

100mV
-100mV
□ V(QMOD)

7055

FIG. 7oK

100mV
-100mV
□ V(RX_I)

7055
7054

FIG. 7oL

100mV
-100mV
1.149us   1.160us   1.180us   1.200us   1.220us   1.240us
□ V(RX_Q)

7055
7086

Time

(B) IQDEMOD RELATIONSHIP OF I AND Q RECEIVED DATA DIFFERENTIAL(BOTTOM) AND SINGLE ENDED AFTER DIFF AMP..
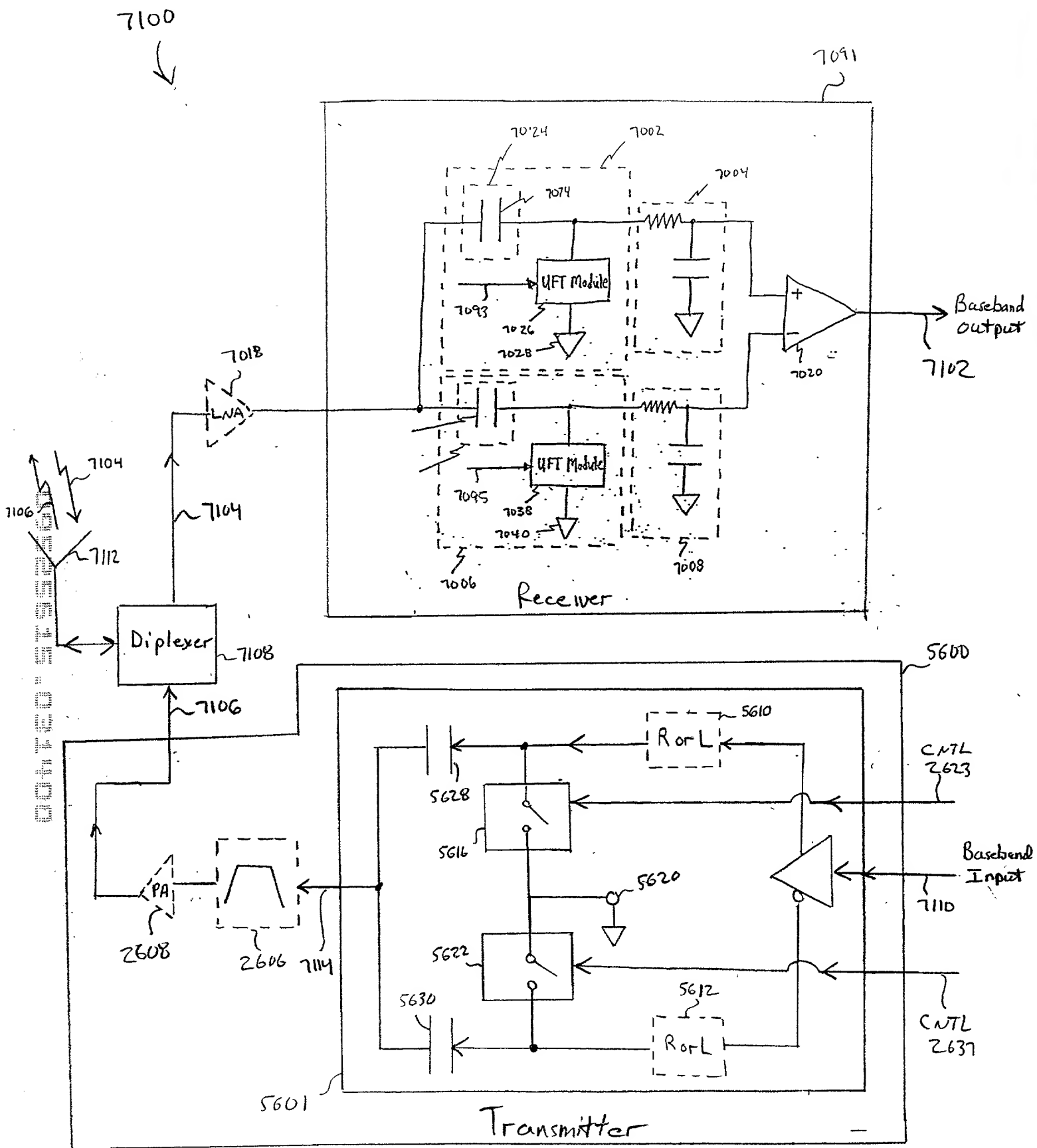

FIG.70M

FIG.70N

FIG.70O

FIG.70P

Page 1

FIG. 70Q

7089

I Baseband
Output Signal
7084

Q Baseband
Output Signal
7086

7092

7075

7073

7087

7085

7083

UFT
Module

7091

First
Control
Signal
7071

7079

UFT
Module

7077

Second
Control
Signal
7069

7082

7072
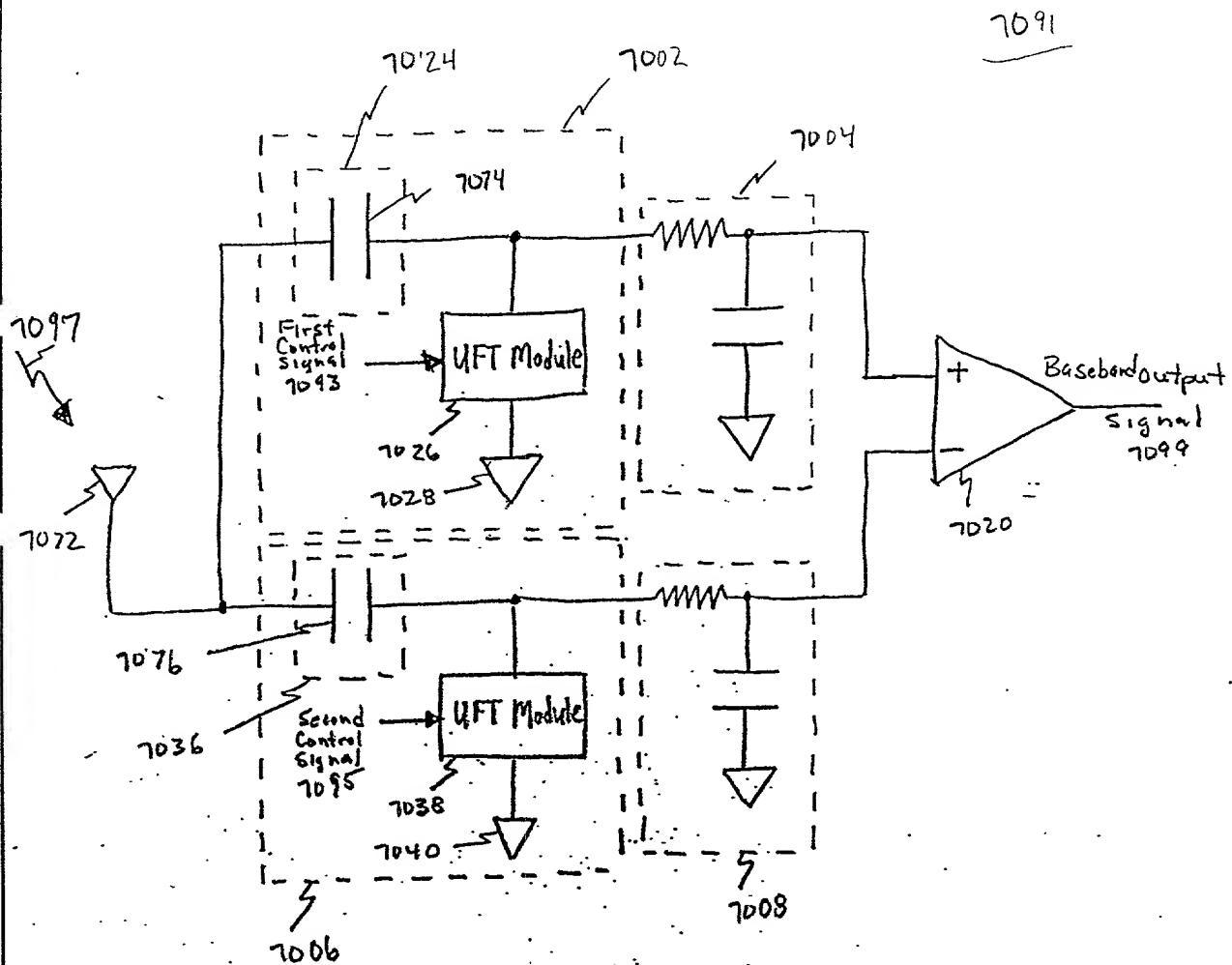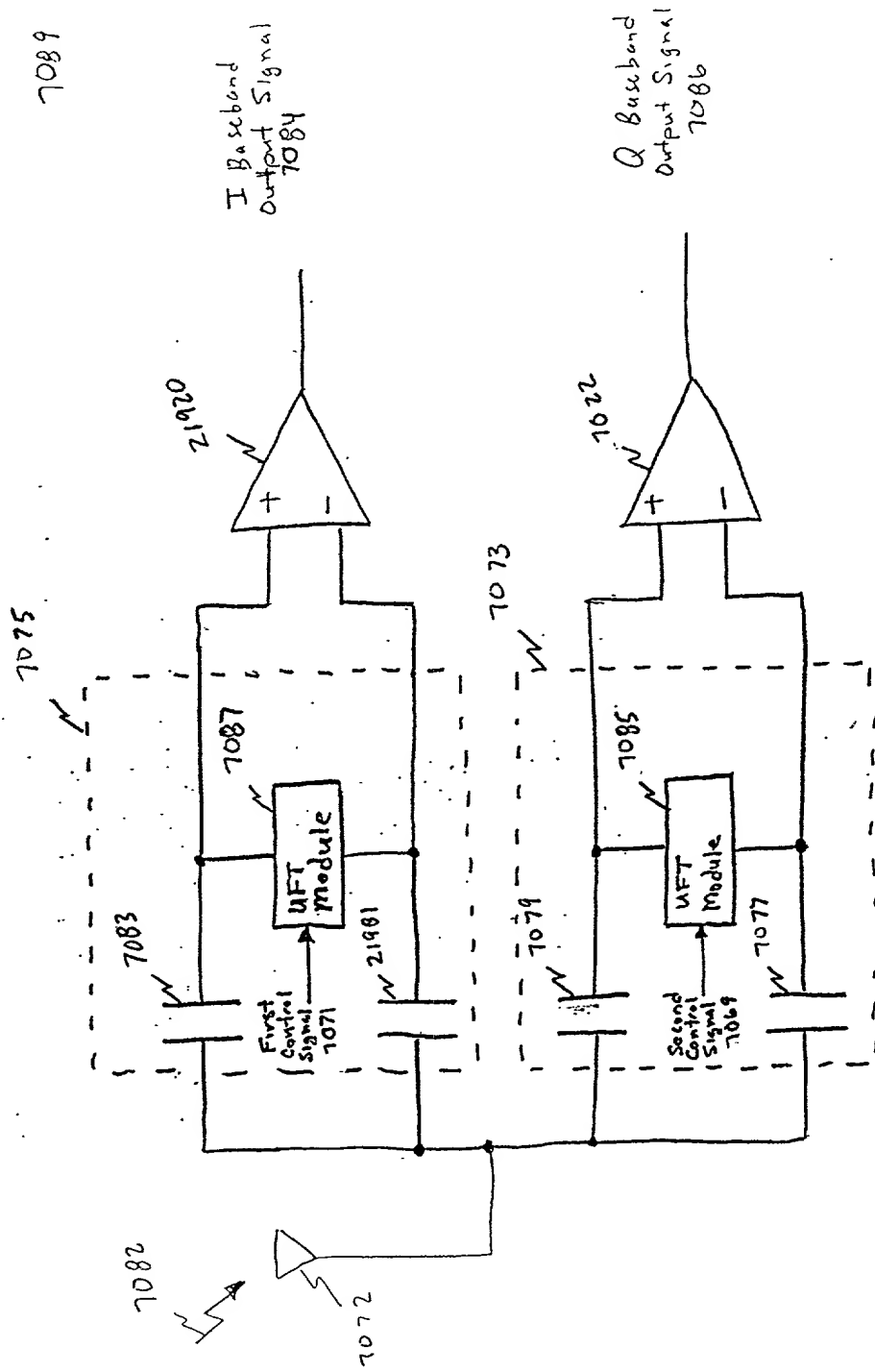
FIG. 70 R

FIG. 71 : Transceiver

Fig. 72

7300

Receive an input baseband signal — 7302

Spread the input baseband signal using I and Q spreading codes resulting in I and Q spread baseband signals — 7304

Filter the I and Q spread baseband signals — 7306

Sample the spread I and Q baseband signals in a balanced and differential manner according to first and second control signals, where the control signals have pulse widths that are established to improve energy transfer to a desired harmonic image — 7308

Amplify the harmonically rich signal — 7310

Select a desired harmonic of interest for transmission — 7312

FIG. 73

7402

Input Signal
7404

Delay 7406

Pulses
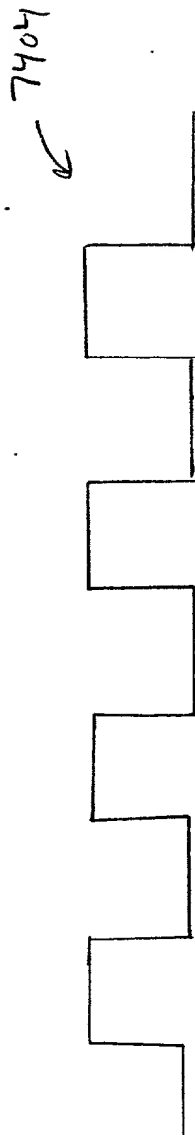7408

Inverter
7410
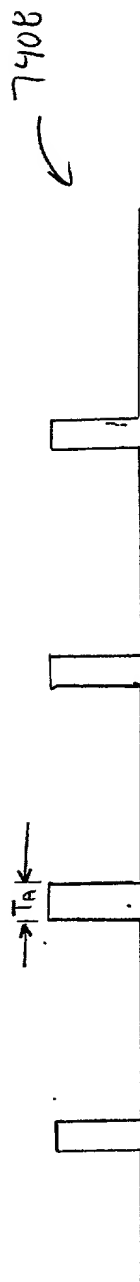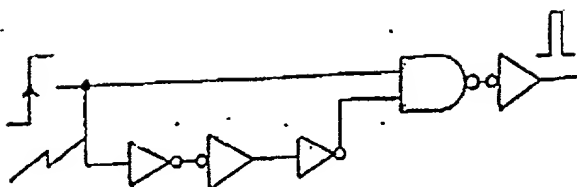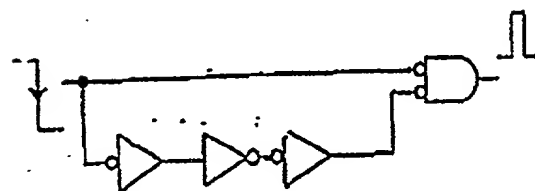
FIG. 74A

7404

7408

T_A

FIG. 74B

FIG. 74C

7412

A. rising edge pulse generator

FIG. 74D

7416

B. falling-edge pulse generator

FIG. 74E